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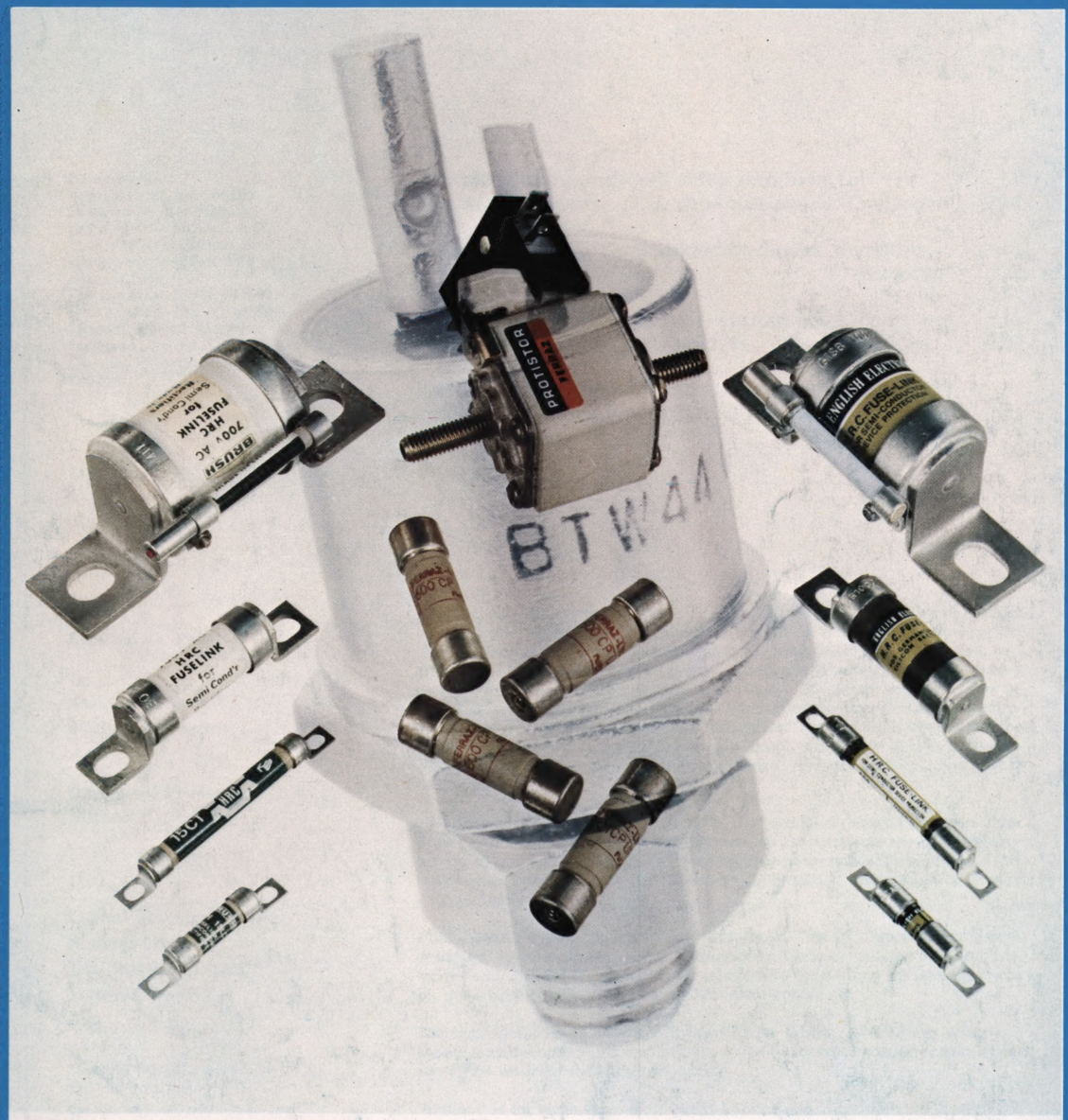

- Complementary push-pull video amplifiers for television receivers
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- Gapped Ferroxcube E-cores for SMPS

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Cover picture:
Typical fuses, specifically designed by fuse manufacturers for the protection of semiconductor devices, are shown here together with a Mullard triac.
For the fuses displayed we wish to thank Brush Fusegear Limited, English Electric Fusegear Limited, and Le Carbone (Great Britain) Limited.

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Complementary push-pull video amplifiers for television receivers

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UDC 621.397.13: 621.375.127 (621.382)

This article describes the design and operation of complementary push-pull video amplifiers having low quiescent current and resultant low power consumption, compared with the conventional class A single-ended video output stages in colour and monochrome receivers. A complete complementary configuration RGB drive amplifier using BF422 and BF423 transistors is described, for use with the TCA800 colour demodulator integrated circuit.

INTRODUCTION

In domestic television receivers, video amplifier stages operating in the class A mode have been used exclusively, chiefly because of their circuit simplicity. Such a class A amplifier driving a video signal into the capacitive load of the picture tube exhibits an asymmetrical transient response. Negative-going edges can be fast because the capacitance is being discharged through the transistor, but the positive-going edges are much slower, being dependent on the time-constant of the load capacitance and the collector load resistor. Overall a.c. feedback only worsens this discrepancy.

The transient performance requirement, therefore, limits the value of the collector load resistor, and consequently in a practical circuit considerable power is wasted. This wastage contributes about 10W (up to 20W under overdrive conditions) to the heat produced in a colour receiver, and increases the cost and physical size of the transistors, heatsinks, and load resistors. By adopting two transistors in each video output stage in a push-pull circuit configuration, the power dissipation can be reduced substantially, minimising the demands upon the transistors and the heatsinks.

A complementary push-pull video amplifier can operate with a power dissipation of approximately 1W under typical picture conditions. Comparing this dissipation with 4 to 6W for a conventional single-ended video stage, a power saving in the complete receiver of some 10 to 15W can be achieved. The complementary video stage requires more components, but these are all small low-power items, and no fabricated heat fins are necessary for the transistors. The space occupied on a printed-wiring board need not therefore be any greater than that for other types of video amplifier.

With present trends to reduce overall power consumption and cabinet ambient temperatures, together with the advances towards data display on domestic television receivers, push-pull video stages have a new significance. In addition to having reduced power consumption, the complementary video amplifier has a much better transient response than the class A single-ended amplifier. Thus, the complementary push-pull video amplifier described in this article is particularly suited to data display applications (see Ref.1).

PUSH-PULL VIDEO DRIVE CIRCUITS

The common feature of push-pull video amplifier circuits (for example, see Fig.1a) is the provision of two active devices connected in series across the h.t. supply. These are driven in such a way that during signal voltage transients, the load capacitance is discharged by transistor TR_2 on negative-going edges of the voltage waveform, and recharged by transistor TR_1 during positive-going edges. Thus a symmetrical transient performance is possible, and because the circuit can be designed so that high peak currents flow in the transistors only during the signal transients, the power consumption of the video stage can be minimised.

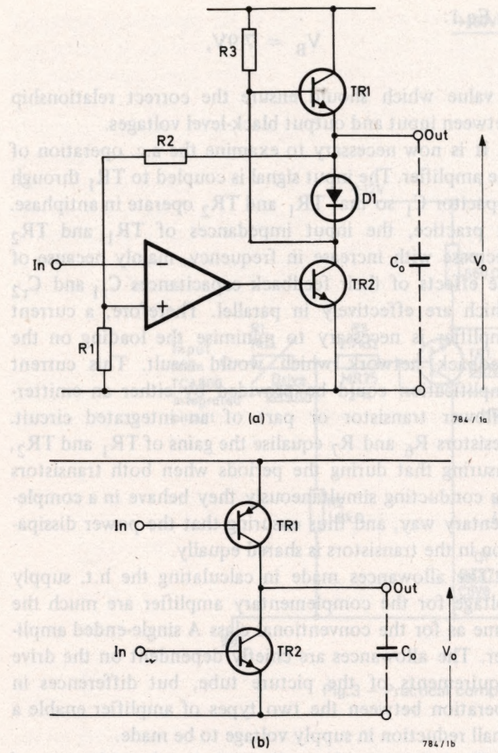

Fig.1 – Video push-pull output stages:
(a) n-p-n plus n-p-n configuration with feedback,
(b) n-p-n plus p-n-p configuration

Two circuit configurations can be used in a push-pull video stage, either two similar transistors in series (such as n-p-n plus n-p-n), or two dissimilar transistors in a complementary series circuit (such as n-p-n plus p-n-p).

N-P-N plus n-p-n configuration

Fig.1a shows the n-p-n plus n-p-n configuration video output stage with feedback included. Transistor TR_2 develops the video signal across the load resistor R_3 in the same way as in a single-ended class A amplifier. The negative-going edges are adequately produced by conduction of TR_2 through diode D_1, and the positive-going edges are produced by conduction of TR_1 operating as an emitter-follower.

When the output signal is negative-going, TR_2 turns on and discharges the load capacitance C_o through D_1. However, when TR_2 turns off, its collector voltage rises, causing D_1 to turn off. Capacitor C_o tends to hold V_o constant until the voltage on the base of TR_1 is sufficiently high to bring TR_1 into conduction. Capacitor C_o is then charged by current flowing through TR_1 which operates as an emitter-follower. Thus a form of crossover distortion occurs each time the output signal direction reverses. The magnitude of this effect is small; that is, only $2 \times V_{be}$. The effect can be largely overcome, and is not normally visible on the picture tube, if sufficient feedback is used to enable the output to be swept rapidly between the two states. This overall feedback (provided by resistors R_1 and R_2) also determines the gain and frequency response.

In practice, the allowable increase in value of R_3, compared with the equivalent resistor in a class A single-ended stage, and also the resultant power-saving, is limited by stray capacitance and the input capacitance of TR_1. Further, TR_1 can be easily damaged by an accidental short-circuit of the output. A more attractive circuit having lower power consumption is provided by an n-p-n plus p-n-p complementary circuit configuration.

N-P-N plus p-n-p complementary configuration

The fundamental n-p-n plus p-n-p complementary configuration output stage is shown in Fig.1b. Transistors TR_1 and TR_2 are driven in such a way as to develop the output signal across the output load capacitance C_o. However, neither the quiescent current nor the stage gain are defined for this circuit. Therefore, variations on the circuit shown in Fig.1b must be used in practice.

Fig.2 shows an n-p-n plus p-n-p configuration output stage. With the aid of Fig.2, the functions of the main components can be described. Because of the potential

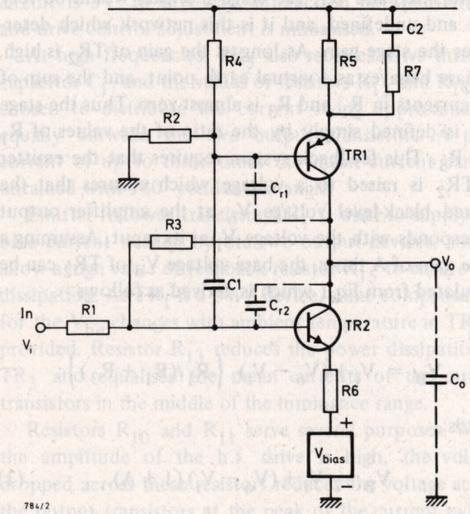

Fig.2 – Video output stage using n-p-n plus p-n-p configuration

difference across the feedback resistor R_3, a current will flow in R_3 at all times, and this current must be provided by conduction of transistor TR_1. Because the drive signal to TR_1 is a.c.-coupled, pure class B operation (zero quiescent current) will not guarantee conduction of TR_1 in the absence of sufficient h.f. content in the input signal.

The simplest solution is to forward-bias TR_1 by the network consisting of resistors R_2, R_4, and R_5. This forward-bias would be sufficient to supply the current required by R_3, the maximum value being approximately equal to $(V_{h.t.} - V_{bias})/R_3$. However, to obtain adequate d.c. stability together with a high a.c. gain for TR_1, resistor R_7 and capacitor C_2 are necessary. Because the a.c. drive peak voltage is small compared with the d.c. voltage across R_5, the collector current of TR_1 will have a substantially-constant mean value.

The magnitude of bias current required has a further constraint due to the need to supply adequate peak currents to charge output load capacitance C_o during positive-going voltage transients under sinusoidal h.f. drive conditions. If this requirement is not fulfilled, that is the conduction angle of transistor TR_2 becomes less than 180°, unequal rise- and fall-times will occur on the output waveform, and the h.f. signal-handling will be adversely affected. The required peak current I_{pk} is proportional to C_o, frequency, and peak-to-peak output signal voltage; and when the conduction angle is not less than 180°, as is required, the mean current in TR_1 must be at least equal to I_{pk}/π. In most practical circuits this mean current value is higher than that required to sustain the current in the feedback resistor R_3.

Without the resistive feedback network consisting of resistors R_1 and R_3, the stage d.c. gain would be very high and undefined, and it is this network which determines the stage gain. As long as the gain of TR_2 is high, its base behaves as a virtual earth point, and the sum of the currents in R_1 and R_3 is almost zero. Thus the stage gain is defined simply by the ratio of the values of R_1 and R_3. This feedback system requires that the emitter of TR_2 is raised to a voltage which ensures that the desired black-level voltage V_o at the amplifier output corresponds with the voltage V_i at its input. Assuming a stage gain of A times, the base voltage V_B of TR_2 can be calculated from Eq.1 which is derived as follows:

$$V_B = V_i + (V_o - V_i)\left\{R_1/(R_1 + R_3)\right\};$$

that is:

$$V_B = V_i + (V_o - V_i)(1 + A). \qquad \ldots (1)$$

If V_i = 3V, V_o = 130V, and A = 25, then, by substitution in Eq.1:

$$V_B = 7{\cdot}9V,$$

a value which should ensure the correct relationship between input and output black-level voltages.

It is now necessary to examine the a.c. operation of the amplifier. The input signal is coupled to TR_1 through capacitor C_1 so that TR_1 and TR_2 operate in antiphase. In practice, the input impedances of TR_1 and TR_2 decrease with increase in frequency, mainly because of the effects of their feedback capacitances C_{r1} and C_{r2} which are effectively in parallel. Therefore, a current amplifier is necessary to minimise the loading on the feedback network which would result. This current amplification could be provided by either an emitter-follower transistor or part of an integrated circuit. Resistors R_6 and R_7 equalise the gains of TR_1 and TR_2, ensuring that during the periods when both transistors are conducting simultaneously they behave in a complementary way, and thus ensuring that the power dissipation in the transistors is shared equally.

The allowances made in calculating the h.t. supply voltage for the complementary amplifier are much the same as for the conventional class A single-ended amplifier. The allowances are chiefly dependent on the drive requirements of the picture tube, but differences in operation between the two types of amplifier enable a small reduction in supply voltage to be made.

The h.f. knee voltage allowance is reduced because of the lower operating currents, and the effect of the h.f. knee voltage is reduced because of the ability of each transistor to increase the speed of recovery from saturation in the other transistor. Further, the allowances for blanking waveform excursion and h.f. knee in TR_2 can overlap, and no allowance needs to be made for the loss of h.t. voltage due to the I_{CBO} which would occur in a single-ended class A stage with a collector load resistor. For a complementary amplifier this current can be absorbed by the complementary transistor. In a typical amplifier, all these factors result in a saving of about 10V after allowance has been made for the bias supply on the emitter of TR_1.

DESIGN OF A VIDEO STAGE FOR USE WITH THE TCA800 INTEGRATED CIRCUIT

When developing a practical video amplifier from the fundamental circuit shown in Fig.2, consideration has to be given to several factors, the first being the drive source of the video signal. Because of the necessity of the feedback over the video stage, resistor R_{15} shown in Fig.3 is required, and in the interest of minimal power dissipation its value should be as high as possible. Ideally, the feedback through R_{15} would be applied to an earlier high-impedance point in the video channel, that is to the

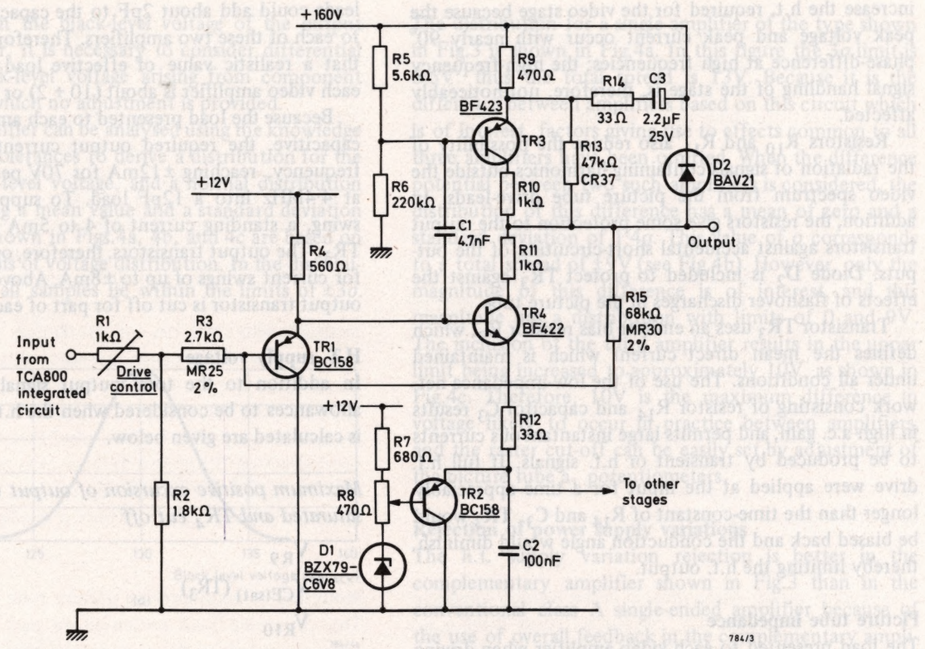

Fig.3 — Practical complementary class B video amplifier

driver integrated circuit, to secure a high loop gain, the best stability of operation, and lowest power dissipation. An integrated circuit for driving complementary video amplifiers is currently under development. The amplifier described below is intended for use with the TCA800 synchronous demodulator and d.c. clamp integrated circuit (Ref.2).

Circuit description

Because the amplifier is designed to be driven from the TCA800 integrated circuit, an emitter-follower transistor is required in each stage to interface with the feedback network configuration. The use of a discrete emitter-follower driver stage is not fundamental to the complementary circuit, however, and with the integrated circuit currently under development for complementary video drive, the discrete emitter-follower is not required.

The complete practical amplifier is shown in Fig.3. At low frequencies, current flows at all times in the output transistors TR_3 and TR_4, and the stage behaves as a class A amplifier, in which TR_4 is driven, and TR_3 and resistor R_{13} form the collector load. The biasing of TR_3 is such that the total current in TR_3 and R_{13} is almost constant. The feedback network consisting of resistors R_3 and R_{15} determines the overall gain. With this feedback network, it is necessary to bias the emitter of TR_4 to approximately 7·5V by means of transistor TR_2 and potentiometer R_8 which removes the common-mode component of spread in the black-level voltages of the three RGB amplifiers.

The values of resistors R_2 and R_3 are proportioned so that no current flows in the drive control potentiometer R_1 at black level, which for the TCA800 integrated circuit is 3V. In this way, interaction between cut-off and drive control adjustment is minimised.

At high frequencies, TR_3 also receives drive through capacitor C_1, and the values of resistors R_{12} and R_{14} are chosen to distribute the current swing approximately equally between the two output transistors. A peak current of up to three times the mean current can be obtained with 180° conduction angle.

Emitter-follower transistor TR_1 is used to supply the base current needed by the two output devices, and to allow a high value of feedback resistor R_{15} to ensure low dissipation. As TR_1 is a p-n-p device, some compensation for the V_{be} changes with ambient temperature in TR_4 is provided. Resistor R_{13} reduces the power dissipation in TR_3 and equalises the mean currents of the output transistors in the middle of the luminance range.

Resistors R_{10} and R_{11} serve several purposes. When the amplitude of the h.f. drive is high, the voltage dropped across these resistors reduces the voltage across the output transistors at the peak of the current swings, thereby reducing the peak dissipation in the transistors. The inclusion of these resistors does not significantly

increase the h.t. required for the video stage because the peak voltage and peak current occur with nearly 90° phase-difference at high frequencies; the high-frequency signal handling of the stage is, therefore, not noticeably affected.

Resistors R_{10} and R_{11} also reduce the possibility of the radiation of signals containing harmonics outside the video spectrum from the picture tube drive-leads. In addition, the resistors give some protection to the output transistors against accidental short-circuiting of the outputs. Diode D_2 is included to protect TR_3 against the effects of flashover discharges in the picture tube.

Transistor TR_3 uses an emitter bias resistor R_9, which defines the mean direct current which is maintained under all conditions. The use of the low-impedance network consisting of resistor R_{14} and capacitor C_3 results in high a.c. gain, and permits large instantaneous currents to be produced by transient or h.f. signals. If full h.f. drive were applied at the input for a time appreciably longer than the time-constant of R_{14} and C_3, TR_3 would be biased back and the conduction angle would diminish, thereby limiting the h.f. output.

Picture tube impedance

The load presented to each video amplifier when driving a picture tube cathode is composed of a resistive part and a capacitive part. The resistive part results from beam current, and is a non-linear resistance which for large-screen picture tubes has a mean value of about 100kΩ. The luminance signals on the three drive-leads to the picture tube will have the same phase and similar amplitude at frequencies above 1MHz. Therefore, the value of the load capacitance C_o on, for example, the drive-lead to the red gun is reduced by the presence of the luminance signals on the drive-leads to the green and blue guns. The load capacitance on the drive-leads to the green gun and the blue gun will be similarly reduced.

The capacitance between adjacent leads will vary as a function of wire length, diameter, spacing, and insulation. Capacitance measurements have been carried out on a typical tv receiver having three 16/0·2 drive-leads, 400mm in length and spaced 8mm apart in a flat ribbon form, with 2mm overall covering in PVC and polyethylene insulation. The measurements show that if the three leads receive equal drive, then the total capacitance between each lead and earth is 10pF. If two of the leads are earthed, the capacitance between the third lead and earth rises by about 6pF. This rise in capacitance corresponds to the value of capacitance between adjacent leads. In practice, the difference in output voltage between any two amplifiers is most likely to lie between 0% and 30% of the total drive voltage to the picture tube, to achieve correct grey scale rendering. If 30% output voltage difference between two amplifiers is assumed, then the current flowing in the 6pF capacitance between adjacent leads could add about 2pF to the capacitance presented to each of these two amplifiers. Therefore, it can be seen that a realistic value of effective load capacitance for each video amplifier is about (10 + 2) or 12pF.

Because the load presented to each amplifier is mainly capacitive, the required output current increases with frequency, reaching ±12mA for 70V peak-to-peak drive at 4·4MHz into a 12pF load. To support this current swing, a standing current of 4 to 5mA is established in TR_3. The output transistors, therefore, operate in class A for current swings of up to ±8mA. Above this level, each output transistor is cut off for part of each cycle.

H.T. supply voltage

In addition to the total output signal excursion, the allowances to be considered when the h.t. supply voltage is calculated are given below.

Maximum positive excursion of output waveform, TR_3 saturated and TR_4 cut off

V_{R9}	2·0V
$V_{CE(sat)}$ (TR_3)	0·5V
V_{R10}	2·0V
Total	4·5V

(No h.f. knee allowance need be made here for transistor TR_3 because no appreciable distortion will occur on the blanking waveform.)

Maximum negative excursion of output waveform, TR_4 saturated and TR_3 conducting

V_{R11}	4·5V
$V_{CE(sat)}$ (TR_4)	0·5V
V_{bias} (V_e, TR_4)	7·5V
V_{knee} (h.f.) (TR_4)	10·0V
Total	22·5V

The above totals must be added to the required output drive voltages given below.

Black-to-white drive	100V
Blanking	15V
Brightness range	20V
Total	135V

Therefore, the required h.t. voltage is (135 + 27) or 162V. In practice, an h.t. voltage of 160 to 165V is satisfactory.

Tolerances of output signal black level

The common-mode bias adjustment provided by R_8 and TR_2 in Fig.3 is described under 'Circuit description'. This adjustment eliminates the need to allow for common-mode spreads in the black-level voltage of the output signals. However, it is necessary to consider differential spreads of black-level voltage arising from component tolerances, for which no adjustment is provided.

A single amplifier can be analysed using the knowledge of component tolerances to derive a distribution for the spread in black-level voltage, and a normal distribution will result having a mean value and a standard deviation σ. The curves shown in Figs.4a, 4b, and 4c are based on computer analysis of voltage distribution. In the distribution, 99·7% of all samples lie within the limits of ±3σ.

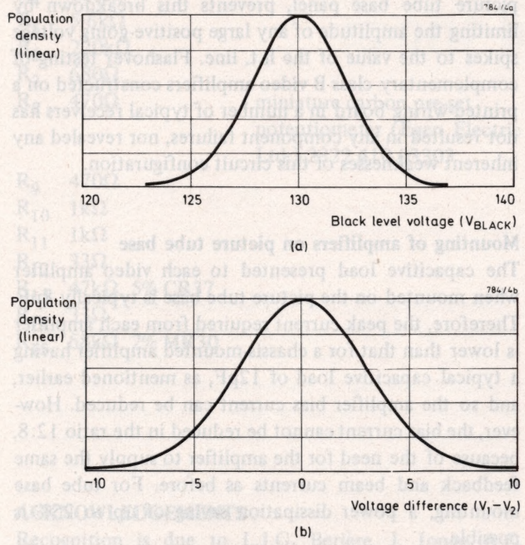

Fig.4 — Spreads in black level voltage for amplifier of type shown in Fig.3, based on computer analysis of voltage distribution:
(a) population density against black level voltage for a single amplifier (common components removed),
(b) population density against black level voltage for two amplifiers,
(c) population density against voltage difference for three amplifiers

The distribution for a single amplifier of the type shown in Fig.3 is shown in Fig.4a. In this figure the 3σ limit is 6·5V: thus the total spread is 13V. Because it is the difference between amplifiers based on this circuit which is of interest, factors giving rise to effects common to all three amplifiers have been omitted. When the difference potential between two such amplifiers is considered, the distribution of this difference has a mean of zero and a standard deviation of 1·4σ. This value of σ corresponds to a total spread of ±9V (see Fig.4b). However, only the magnitude of this difference is of interest, and this magnitude has a distribution with limits of 0 and 9V. The inclusion of the third amplifier results in the upper limit being increased to approximately 10V, as shown in Fig.4c. Therefore, 10V is the maximum difference in voltage likely to occur in practice between amplifiers, and the raster cut-off can be easily set by adjustment of the picture tube a_1 potentiometers.

Rejection of power supply variations

The h.t. supply variation rejection is better in the complementary amplifier shown in Fig.3 than in the conventional class A single-ended amplifier because of the use of overall feedback in the complementary amplifier. The l.t. supply rejection is optimised by the choice of the values of resistor R_7 and potentiometer R_8, and the voltage for diode D_1. As a result, in the nominal amplifier the bias voltage on the emitter of TR_4 tracks with the black-level voltage supplied by the TCA800 driver integrated circuit. The typical results obtained for 5% variation in supply voltage are given below:

160V h.t. supply (+8V)	0·75V variation,
12V l.t. supply (+0·6V)	2V variation.

Signal handling, rise-time, and frequency response

Fig.5 shows the typical relationship between maximum peak-to-peak output voltage and frequency for the practical complementary class B video amplifier shown

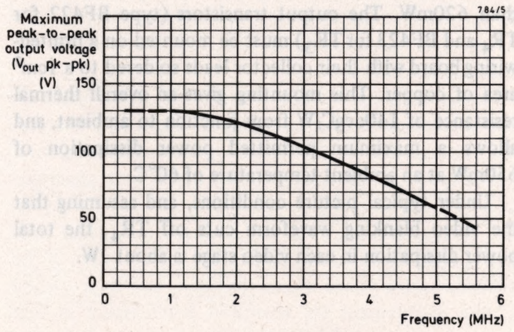

Fig.5 — Maximum peak-to-peak output voltage V_{out}pk-pk against frequency (MHz) for amplifier shown in Fig.3

in Fig.3. The significant roll-off at high frequencies is deliberate, and saves power dissipation without impairing picture quality, assuming that a chroma signal trap is used in the luminance channel, and that a 100V peak-to-peak picture tube drive signal at 4MHz is therefore not required.

The rise-time, determined by the peak current available from the amplifier, is less than 100ns for a 100V step output. The rise-time is similar for positive- and negative-going waveform edges, with overshoot of less than 4%. The overshoot can be optimised by altering the stray capacitance across R_{15}, and on the laboratory prototype printed-wiring board some extra print track provides the necessary capacitance. Asymmetry of step response arises if the value of resistor R_4 is made too large, and this results in limitation of the drive current to the output stages on a black-to-white transition.

With a load capacitance of 12pF, the bandwidth at the −3dB points is approximately 8MHz with reference to a 1MHz output signal of amplitude 10V peak-to-peak.

Power dissipation

The highest power dissipation in either output transistor in Fig.3 occurs under d.c. conditions when there is no superimposed a.c. signal. This dissipation is maximum for TR_3 at peak-white level, and for TR_4 as the output voltage approaches the h.t. value. In both instances, the maximum power dissipation under the worst combination of component tolerances is 620mW.

The power dissipation in each output transistor under typical picture conditions is about 300 to 500mW. Under conditions of overdrive and clipping, with a continuous 5MHz grating displayed, the power dissipation is 530mW for TR_3 and 570mW for TR_4: at lower frequencies, the power dissipation is less. These figures assume continuous operation, and make no allowance for blanking. If the blanking cuts off the transistors, the dissipation figures will fall by 18%. However, if cut-off does not occur, TR_4 reaches maximum dissipation during blanking. Therefore for safe operation under the worst conditions, the transistors must each be capable of dissipating not less than 620mW. The output transistors (type BF422 for TR_4 and BF423 for TR_3) must be mounted on a printed-wiring board with their collector leads soldered to a 1cm² area of copper. This mounting gives an overall thermal resistance of 140degC/W from junction to ambient, and allows a maximum permitted power dissipation of 650mW at an ambient temperature of 60°C.

Under typical picture conditions, and assuming that the video blanking waveform cuts off TR_4, the total power dissipation in each video stage is about 1W.

Picture tube flashover safety

E.H.T. discharges in the picture tube can result in positive-going voltage spikes on the picture tube cathodes. The operation of TR_4 is similar to the operation of transistors used in conventional video amplifiers, and experience has shown that no special flashover problems occur provided that the usual precautions are taken. Transistor TR_3, however, requires some further protection because a large-amplitude positive-going pulse would cause forward conduction of its collector-base junction, and the base-emitter junction could be broken down by conduction in the reverse direction. Diode D_2, in conjunction with the use of protection resistors on the picture tube base panel, prevents this breakdown by limiting the amplitude of any large positive-going voltage spikes to the value of the h.t. line. Flashover testing of complementary class B video amplifiers constructed on a printed-wiring board in a number of typical receivers has not resulted in any component failures, nor revealed any inherent weaknesses of this circuit configuration.

Mounting of amplifiers on picture tube base

The capacitive load presented to each video amplifier when mounted on the picture tube base is typically 8pF. Therefore, the peak current required from each amplifier is lower than that for a chassis-mounted amplifier having a typical capacitive load of 12pF, as mentioned earlier, and so the amplifier bias current can be reduced. However, the bias current cannot be reduced in the ratio 12:8, because of the need for the amplifier to supply the same feedback and beam currents as before. For tube base mounting, a power dissipation saving of up to 25% is possible.

Monochrome application

The benefits offered by the complementary configuration also apply where monochrome picture tubes are to be driven, and in receivers designed for battery operation the resultant power-saving is attractive. Depending on the characteristics of the available video signal, the bias voltage for TR_4 would probably still be necessary. The function of TR_2 in a colour receiver is to prevent cross-talk between the RGB amplifiers. Therefore TR_2 will not be required in a monochrome receiver. A simplified form of bias adjustment could be used if necessary. A video emitter-follower transistor commonly comes after the video detector in monochrome receivers, and this transistor could supply the low-impedance drive for the complementary stage.

COMPONENTS LIST

A list of components for the practical complementary class B video amplifier is given below.

Resistors

All resistors are type CR25 ±5% except where stated.

R_1	1kΩ	miniature carbon pre-set potentiometer (Egen Electric Ltd.) 2322 410 03304
R_2	1·8kΩ	
R_3	2·7kΩ, 2% MR25	
R_4	560Ω	
R_5	5·6kΩ	
R_6	220kΩ	
R_7	680Ω	
R_8	470Ω	miniature carbon pre-set potentiometer (Egen Electric Ltd.) 2322 410 03303
R_9	470Ω	
R_{10}	1kΩ	
R_{11}	1kΩ	
R_{12}	33Ω	
R_{13}	47kΩ, 5% CR37	
R_{14}	33Ω	
R_{15}	68kΩ, 2% MR30	

Capacitors

C_1	4·7nF, 400V 347 51472
C_2	100nF, 250V C280AE/P100K
C_3	2·2μF, 25V 122 56228

Transistors

TR_1	BC158
TR_2	BC158
TR_3	BF423
TR_4	BF422

Diodes

D_1	BZX79-C6V8
D_2	BAV21

ACKNOWLEDGEMENTS

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Fuse protection of semiconductor diodes, thyristors, and triacs

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UDC 621.316.923: 621.382

Techniques for matching the characteristics of fuses to the surge current capabilities of diodes, thyristors, and triacs are described. The effects of moderate overload conditions and high-current faults, together with the relationship of fuse arc voltage to peak reverse voltage, are considered. Examples of fuse selection for the BTW92 thyristor, based on energy let-through (I^2t) coordination are given.

INTRODUCTION

The article describes the principles of fuse protection of semiconductor devices. It does not cover every aspect of fusing, because many practical fusing techniques have already been established for many years. The article, therefore, restricts itself to the coordination of the fuse to the semiconductor device, and includes the principles of the short-circuited power line, fuse construction, and fuse characteristics.

Much has been written over the last thirty years on the characteristics and operation of fuses. In particular, the introduction of the so-called 'current-limiting fuse' has allowed the effective protection of electrical apparatus against the effects of a complete short-circuit. Previously, the current-limiting fuse was normally associated with heavy-duty electrical equipment. The introduction of the semiconductor power diode, thyristor, and triac created a new requirement for improved performance in fuse protection from short-circuit faults, because of the low overload capability of semiconductor devices.

The fundamental protection of semiconductor devices against high-current faults is achieved by the limitation of energy let-through I^2t, expressed in A^2s. The let-through of the fuse is compared with the I^2t withstand capability of the device as given in the semiconductor manufacturer's published data. There is evidence to indicate that the peak current let-through of the fuse, the wave-shape, and the time at which the peak occurs after the commencement of the short-circuit should correspond to the peak current and time withstand of the semiconductor device. However, this part of the process of matching a fuse to a semiconductor device is under continuous development.

SHORT-CIRCUITED A.C. POWER LINE

It is clear that a fuse must give reliable protection over a wide variety of overload conditions to satisfactorily protect the circuit and devices. In many examples of circuit protection, fuses are used in conjunction with circuit breakers. In this arrangement, the circuit breaker deals with moderate overloads, and the fuse deals with a high-current fault resulting from a circuit breakdown. For example, curves of surge current I_{FSM}(r.m.s.) against time are shown in Fig.1 for the BYX98 diode protected by an English Electric GSA10 fuse and a mechanical circuit breaker. It can be seen in Fig.1 that the fuse protects the diode and the circuit breaker against high-current surges of less than about 30ms duration, whereas the circuit breaker protects the diode and the fuse against low-current surges of longer duration. Fusing is of

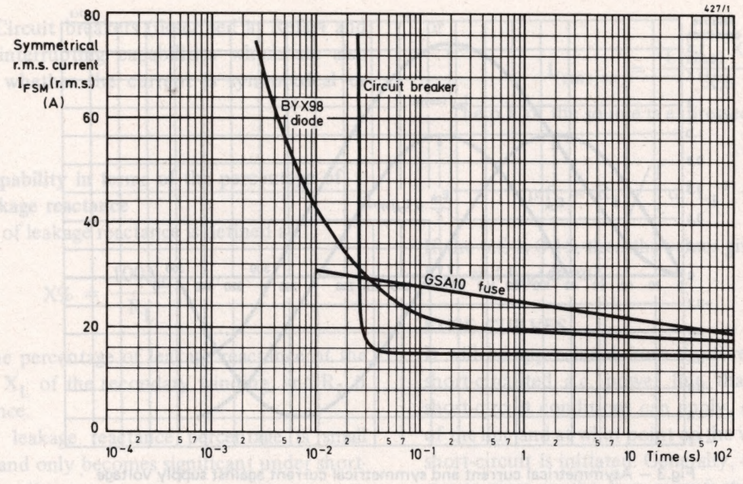


Fig.1 — Curves of surge current I_{FSM} (r.m.s.) against time for BYX98 diode protected by English Electric GSA10 fuse and mechanical circuit breaker

course required for d.c. as well as a.c. supplies, but most manufacturers derate a suitable a.c. fuse for this purpose, as described later.

Fig.2 represents a short-circuit occurring on a single-phase a.c. power line. The inductance L represents the inductive component of the line, including the leakage inductance of the substation transformer. The resistance R represents the resistive component. In high-power installations, the value of R is very low, and a short-circuited line is normally highly inductive. The ratio $\omega L/R$ has been standardised by the American National Electrical Manufacturers Association to a value of 6·66. This standardised value corresponds to a power factor (p.f.) of 0·15 (see Ref.1) for fuse and circuit breaker performance data. Similar standardisations apply in the United Kingdom and in other European countries.

The general equation for the instantaneous current i(t) is given below:

$$i(t) = \frac{E_{pk}}{Z}\left\{\sin(\omega t + \theta - \phi) - e^{-kt}\sin(\theta - \phi)\right\}, \quad \ldots(1)$$

where: E_{pk} = peak value of the sinewave voltage,
Z = impedance of the line,
θ = angle at which the short-circuit occurs relative to the sinewave voltage zero,
ϕ = $\tan^{-1}\omega L/R$,
k = R/L.

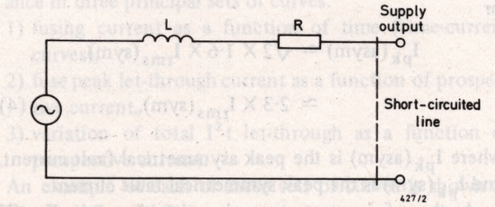


Fig.2 — Occurrence of short-circuit in a single-phase power line

Eq.1 consists of a steady-state term:

$$\frac{E_{pk}}{Z}(\sin\omega t + \theta - \phi),$$

and a transient term:

$$\frac{E_{pk}}{Z}\left\{-e^{-kt}\sin(\theta - \phi)\right\}.$$

When θ is equal to ϕ, that is where a short-circuit occurs at the lag-angle of the line, the transient term is equal to zero. This condition represents the 'steady-state' current-against-voltage relationship of an a.c. supply. The steady-state current i(t) is given by:

$$i(t) = \frac{E_{pk}\sin\omega t}{Z}. \quad \ldots(2)$$

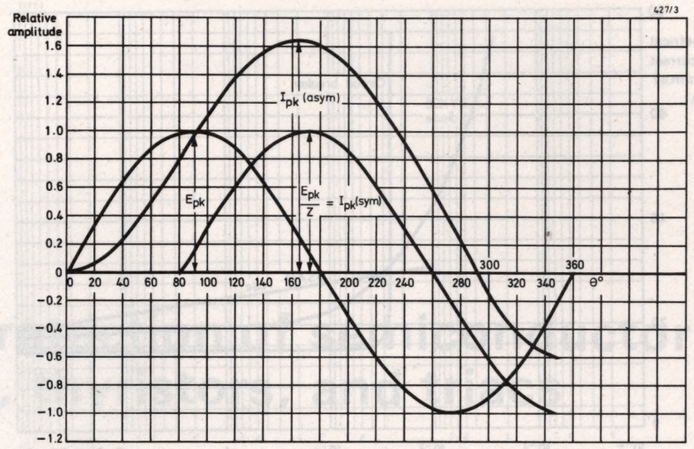


Fig.3 — Asymmetrical current and symmetrical current against supply voltage during one cycle

Fig.3 shows the waveforms of voltage, symmetrical current, and asymmetrical current derived from Eq.1 for a p.f. of 0·15. As indicated in Fig.3:

$$I_{pk}(\text{asym}) \simeq 1{\cdot}6 \times I_{pk}(\text{sym}), \qquad \ldots(3)$$

or

$$I_{pk}(\text{asym}) \simeq \sqrt{2} \times 1{\cdot}6 \times I_{rms}(\text{sym}),$$

$$\simeq 2{\cdot}3 \times I_{rms}(\text{sym}), \qquad \ldots(4)$$

where I_{pk}(asym) is the peak asymmetrical fault current, and I_{pk}(sym) is the peak symmetrical fault current.

As the p.f. increases towards unity, the peak value of the asymmetrical transient current decreases, and the asymmetrical and symmetrical peak currents tend to become in phase with the generated sinewave voltage.

Mains supply source with transient suppression filter

In many instances where thyristors are used in bridge circuit configurations direct from the mains supply, transient suppression filters are required to suppress spikes on the mains voltage waveform. These voltage spikes can cause spurious dV/dt or V_{BO} triggering. An example of a transient suppression filter connected to the supply line is shown in Fig.4, which is reproduced from Ref.2. The R_2, L_2, and C_1 circuit is chosen to be a nearly critically damped system by suitable choice of the three component values. Resistor R_3 is a high-value component which assists in the discharge of capacitor C_1. If a complete short-circuit occurs on the output side of the filter, the inductance L_2 and its associated resistance r_2 becomes part of the power line in terms of the prospective current generated. In high-power installations, the p.f. of the supply line is almost certain to be known, and the values of L_2 and r_2 may be added to the values of L_1 and R_1 for calculation purposes.

In practical terms, the significance of the symmetrical and asymmetrical short-circuit is the way in which the initial rate of rise of current affects the operation of the protective device. Where a fuse is the protective device, Ref.3 shows that there may be a difference in the peak current let-through under short-circuit conditions, depending on whether the current is symmetrical or

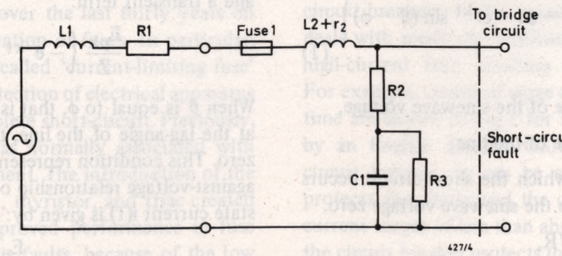


Fig.4 — Transient suppression filter connected to supply line

asymmetrical. Circuit breakers (described in Refs.4 and 5) may have interrupting capabilities which are also dependent on whether the current is symmetrical or asymmetrical.

Short-circuit capability in terms of the percentage of transformer leakage reactance

The percentage of leakage reactance is defined as:

$$X\% = \frac{100X_L}{R_L},$$

where X% is the percentage of leakage reactance of the total reactance X_L of the secondary winding, and R_L is the load resistance.

Usually the leakage reactance percentage is small (typically 2%) and only becomes significant under short-circuited load conditions.

The nominal volt-amp rating VA_{nom} of the transformer is given by:

$$VA_{nom} = E_{rms}\, I_{L(rms)},$$

$$= E^2_{rms}/R_L. \qquad \ldots(5)$$

The short-circuit VA rating VA_{sc} is given by:

$$VA_{sc} = E^2_{rms}/X_L. \qquad \ldots(6)$$

From Eq.6:

$$VA_{sc} = \frac{VA_{nom} \times 100}{X\%}, \qquad \ldots(7)$$

or

$$I_{(rms)sc} = \frac{I_{L(rms)} \times 100}{X\%}. \qquad \ldots(8)$$

The p.f. of the source is expressed as:

$$\text{p.f.} = R_1 \Big/ \left[\omega^2 L_1{}^2 + R_1{}^2\right]^{\frac{1}{2}}. \qquad \ldots(9)$$

If the p.f. is 0·15, then the values given in Eq.4 apply for I_{rms} and I_{pk}(asym).

FUSE CURVES

It will be appreciated from the foregoing section on the short-circuited a.c. power line that a great variety of short-circuit conditions can apply, depending on the p.f. of the line and at what point on the voltage waveform the short-circuit is initiated. Generally, the fuse performance curves given in the fuse manufacturer's published data are derived from worst-case conditions (see Ref.1). It follows that the conditions under which a fuse clears in a particular situation will probably produce less stress in the device or equipment to be protected than is indicated by the fuse performance curves.

It has been normal practice to present fuse performance in three principal sets of curves:

1) fusing current as a function of time (time-current curves),
2) fuse peak let-through current as a function of prospective current,
3) variation of total I^2t let-through as a function of prospective current.

An example of each of these sets of curves is shown in Figs.5, 6, 7a, and 7c.

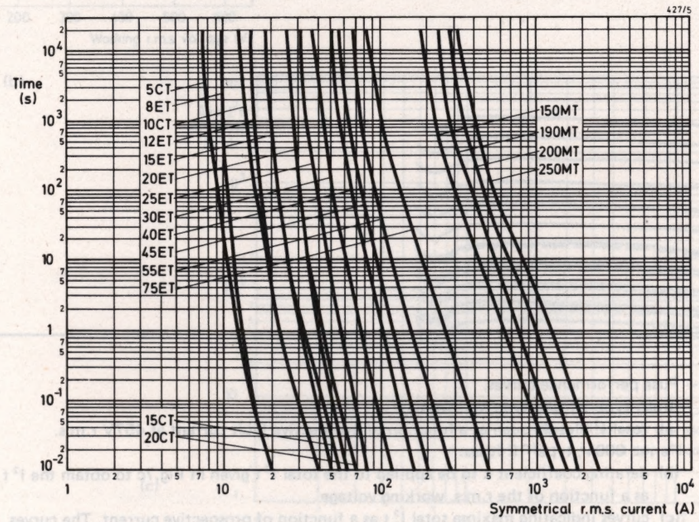


Fig.5 — Time-current curves for Brush type ET and type MT fuses

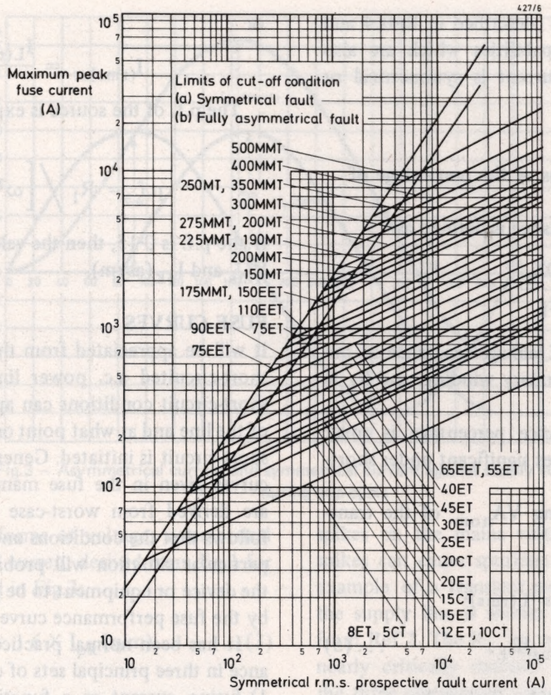
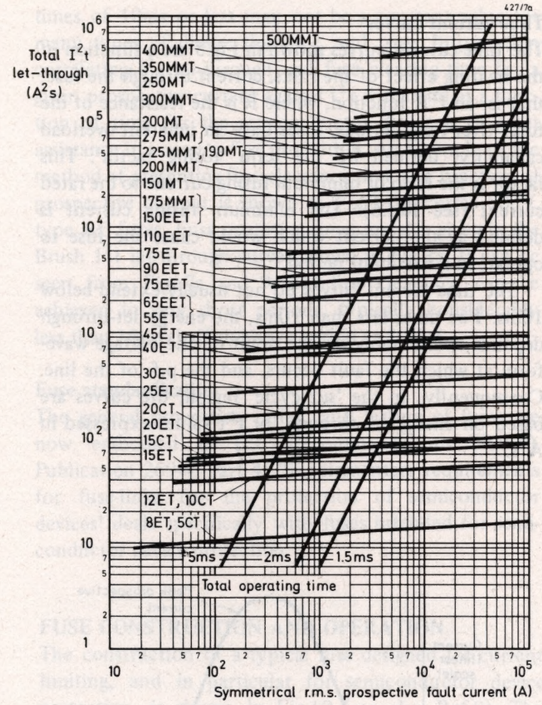
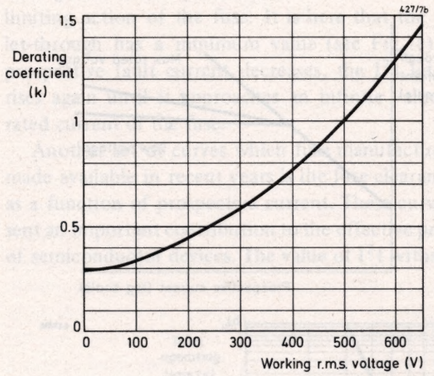


Fig.6 — Curves of fuse maximum peak current as a function of prospective fault current for Brush type ET and type MT fuses (cut-off characteristics at 457V r.m.s.)

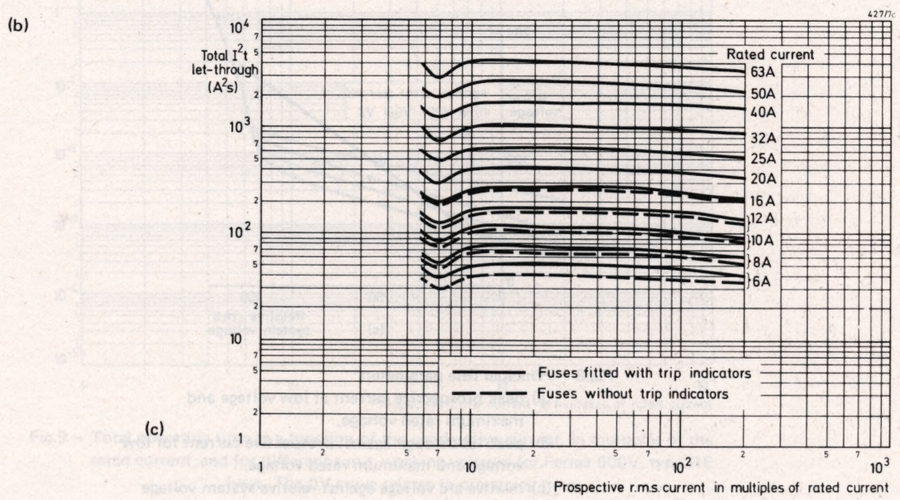
Fig.7 — Fuse performance curves.
Brush type ET and type MT fuses:
(a) total I^2t let-through as a function of prospective fault current at 457V r.m.s.
Ferraz 600V, type RE fuses:
(b) derating coefficient k to be applied to the total I^2t given in Fig.7c to obtain the I^2t as a function of the r.m.s. working voltage
(c) curves indicating maxima total I^2t as a function of prospective current. The curves are expressed in multiples of the rated current for operation under 500V at 50Hz



(a)



(b)



(c)

Time-current curves

The time-current curves shown in Fig.5 are a function of the heating effect of the r.m.s. current through the fuse; that is, an i^2R function, where R is the resistance of the fuse. Over long periods, fuses have an inherent overload capability, defined by the term 'fusing factor'. This factor is the ratio of minimum fusing current to the rated current (see Ref.6). The minimum fusing current is defined as the current which would cause the fuse to operate in a four-hour period.

The time-current curves do not usually extend below 10ms. For times less than 10ms, the energy let-through depends considerably on the point on the voltage waveform at which the fault occurs, and the p.f. of the line. Consequently, in the 'sub-cycle' region, the curves are based on energy let-through, or I^2t values expressed in A^2s.

Peak let-through current

The fuse peak let-through is usually plotted from two boundary ordinates, signifying a symmetrical fault and a fully-asymmetrical fault, as shown in Fig.6. The maximum peak current characteristic for a rated fuse is derived from a multiplicity of circuit conditions (Ref.1). The peak current passed by a fuse is somewhat influenced by the fuse arc voltage characteristic and the system voltage, as indicated in Figs.8a and 8b. The relative arc voltage of the fuse against the relative system voltage is shown in Fig.8c. Therefore, the fuse melting time and the current flow in the pre-arcing interval do not accurately indicate the maximum peak let-through. In addition, a secondary effect concerning low-current fuses (Ref.7) is the modification of pre-arcing current to a lower rate of rise of fault current. This modification is due to the increased resistance in the line, caused by the high-temperature

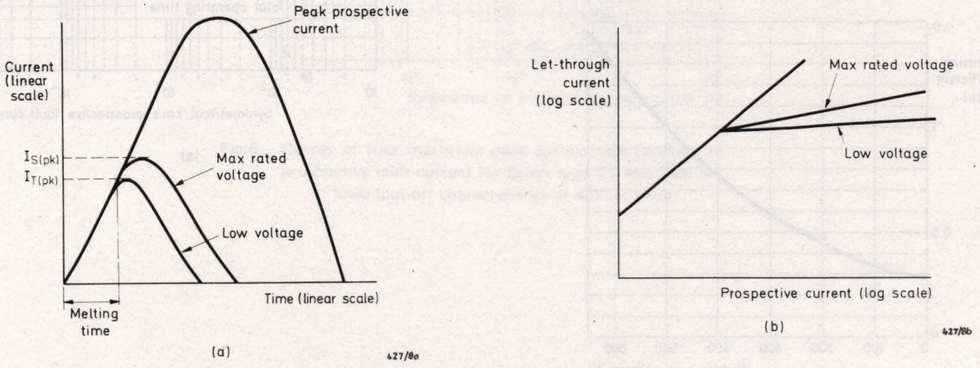


Fig.8 — Principal fuse parameters:
(a) peak prospective current at low voltage and maximum rated voltage,
(b) peak let-through against prospective current for low voltage and maximum rated voltage,
(c) relative arc voltage against relative system voltage

fuse element immediately before the melting point of the silver element is reached at 960°C.

I^2t let-through curves

Performance curves are shown in Fig.7a for Brush type ET and type MT fuses, and in Figs.7b and 7c for Ferraz 600V type RE fuses. The curves indicate maximum I^2t values for a given supply voltage and a low-p.f. circuit. As described later, the I^2t let-through curves represent the sum of the melting I^2t and the arcing I^2t of a particular fuse. The arcing I^2t is particularly dependent on the supply voltage, and fuse manufacturers include voltage derating graphs in their published data. An example of such a derating graph is shown in Fig.7b, subsidiary to the main graph of I^2t let-through against prospective fault current (see Fig.7c). The subsidiary graph is used to derate the total I^2t let-through of the fuse by a fractional factor (k in Fig.7b) as the supply voltage decreases from the maximum-rated value of the fuse. Other manufacturers give I^2t curves for specific test voltages (for example, see Fig.7a). The starting point of an I^2t let-through curve usually corresponds to the onset of current limiting action of the fuse. It is here that the total I^2t let-through has a minimum value (see Fig.7c). As the prospective fault current decreases, the I^2t let-through rises again until it approaches an infinite value for the rated current of the fuse.

Another set of curves which fuse manufacturers have made available in recent years is the fuse clearance times as a function of prospective current. These curves represent an important contribution to the effective protection of semiconductor devices. The value of I^2t withstand for times of 10ms or less may not be a constant value for many types of diode, thyristor, and triac. Information correlating I^2t let-through and fuse clearing time for a given prospective current against I^2t withstand as a function of time for the semiconductor device is of great assistance in assessing fuse protection. An example of the method of presenting fuse clearance time as a function of prospective current is shown in Fig.9 for Ferraz 600V, type RE fuses. Fuse operating times are also given in the Brush I^2t let-through curves shown in Fig.7a. It can be seen from Figs.7a and 9 that fuse clearance can be achieved in very short periods, typically considerably less than 10ms (half-sinewave period at 50Hz).

Fuse standardisation

The general properties, rating, and testing of fuses are now embodied in IEC Recommendations (Ref.8). Publication 269-4, Part 4: 'Supplementary requirements for fuse-links for the protection of semiconductor devices' deals specifically with fuses intended for semiconductor device protection.

FUSE CONSTRUCTION AND OPERATION

The construction of a typical fuse designed for current limiting, and in particular for semiconductor device protection, is shown in Fig.10 (see also Ref.9). The fusing element is usually made of silver to ensure very low ohmic resistance. Typical shapes of fuse elements are shown in Figs.11a and 11b. V-shaped notches are made in the element to produce a number of constrictions, and the fusing action takes place at one or more of

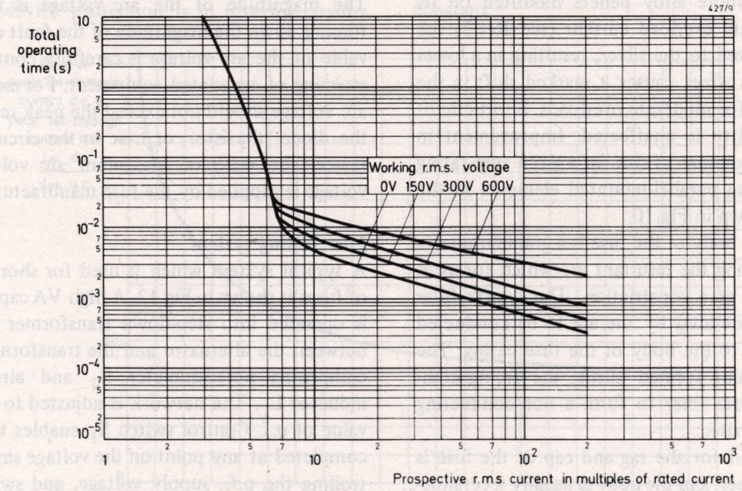


Fig.9 — Total operating time as a function of the prospective current, in multiples of the rated current, and for different r.m.s. working voltages for Ferraz 600V, type RE fuses. The 0V curve relates to pre-arcing time

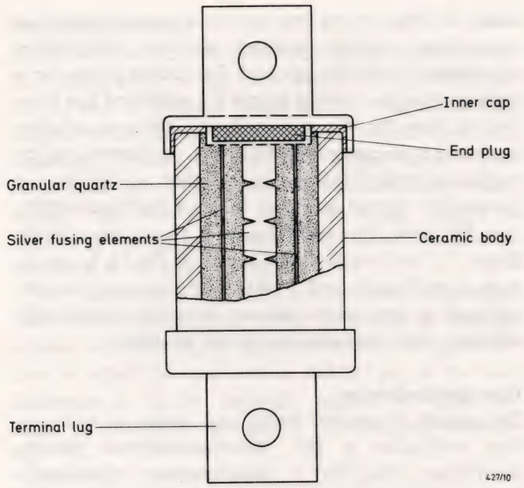


Fig.10 — Cut-away drawing of typical fuse for semiconductor protection

these constrictions. The v-shaped notch is chosen instead of rectangular- or semicircular-shaped notches for two principal reasons. First, it combines minimum heat generation with maximum heat dissipation at the minimum cross-section. Consequently, the v-shaped section can carry the greatest overload current. Second, elements with v-shaped notches show a considerably reduced I^2t (arcing) tendency than elements with notches of other shapes. The element shown in Fig.11a is used primarily for the short-circuit protection of semiconductor devices. The element in Fig.11b is intended for industrial use and may have one or more alloy pellets mounted on its surface. On moderate overload current (see Ref.7) the pellets become alloyed to the silver, resulting in a lower melting point. This effect causes a marked shift in the time-current curves for moderate overloads. Short-circuit interruption capability is unaffected. Improvement in performance and economy of size for a given amp-rating is obtained by using parallel-mounted elements in the same housing as shown in Fig.10.

Contained in the body of the fuse is a granular quartz filler for extinguishing the resultant arc which forms as the element breaks at a constriction. The quartz filler enables the heat generated by the arc to be conducted axially and radially to the body of the fuse casing. The resultant silver vapour formed during the arcing combines with the quartz filler to form a non-conducting material called fulgurite.

The material used for the tag and cap of the fuse is usually brass or copper, and the body is usually a ceramic-based material which will withstand high thermal shock.

At sufficiently high short-circuit currents, the element melts. The theoretical energy required to melt the

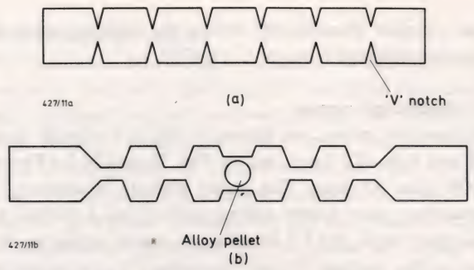


Fig.11 — Typical shapes of elements used in fuses for:
(a) semiconductor protection,
(b) industrial use

element at one of the constrictions formed by a notch is given by:

$$E_j \text{ (joules)} = \int_0^{t_1} i^2 R \, dt, \qquad \ldots (10)$$

where R is the mean fuse resistance, and t_1 is the melting time limit (see Ref.2). E_j and R in Eq.10 are combined in one constant K given by:

$$K = E_j/R.$$

Therefore:

$$K = \int_0^{t_1} i^2 \, dt, \qquad \ldots (11)$$

where K is expressed in A^2s.

During the arcing period, the arc voltage can be considerably higher than the mains supply voltage, depending on the element design. The additional voltage is supplied by the trapped inductive energy of the circuit. The magnitude of the arc voltage is instrumental in forcing down the magnitude of the fault current, but the value of the arc voltage is carefully controlled to avoid stressing of associated equipment. For example, the fuse arc voltage should not exceed the peak reverse voltage of the diode, thyristor, or triac in the circuit, and for this reason the ratio of maximum arc voltage to system voltage is supplied by the fuse manufacturer.

Fuse testing system

A typical system which is used for short-circuit testing of fuses is shown in Fig.12. A high VA capacity alternator is operated into step-down transformer T_1. Connected between the alternator and the transformer is a network comprising potentiometer R_1 and air-cored variable inductor L_1. The network is adjusted to set up a known value of p.f. Control switch S_1 enables the circuit to be completed at any point on the voltage sinewave. By controlling the p.f., supply voltage, and switching point, a wide range of fusing conditions can be simulated, from which worst-case conditions can be evaluated for fuse curves.

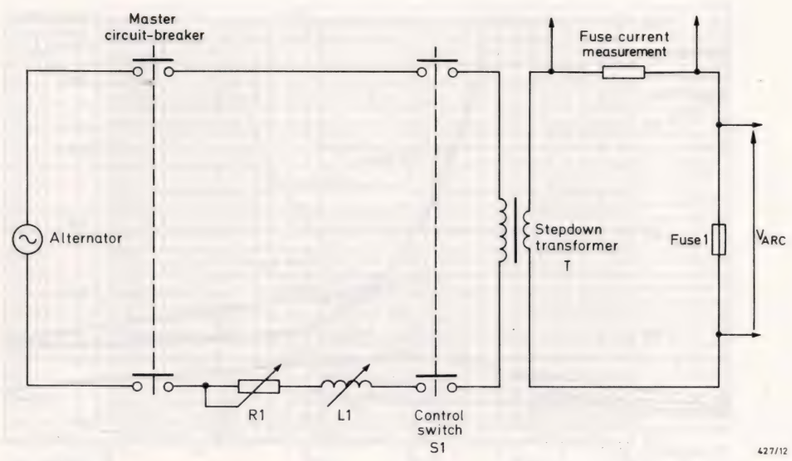


Fig.12 — Typical system used for short-circuit testing of fuses

D.C. OPERATION OF FUSES

Discussion has centred so far on fuses operating on a.c. supplies, and it is in this situation where most fuses are used. Under d.c. conditions there is an absence of voltage zero points, but for high-current fault conditions in d.c. circuits having a low time-constant, fuse clearing times can be similar to those for a.c. circuits. However, for d.c. circuits with lower fault currents and larger time-constants, voltage derating of the fuse will be necessary. Consequently, there is no direct relationship between a.c. and d.c. fusing systems (see Refs.10 and 11).

A specialised d.c. application of fuses intended for semiconductor device protection is in inverter circuits using thyristors. In these circuits, commutation failure due to excessive load current can occur. This type of failure can result in two conducting devices being placed across the d.c. line. Individual fuse protection of each device can be used in a similar manner to branch fusing.

For d.c. circuits with typical time-constants, the peak let-through current of the fuse is less than the peak let-through current for worst-case conditions in a.c. operation. The curve shown in Fig.13 gives an indication of the ratio of d.c. peak let-through current to a.c. peak let-through current as a function of the circuit d.c. time-constant.

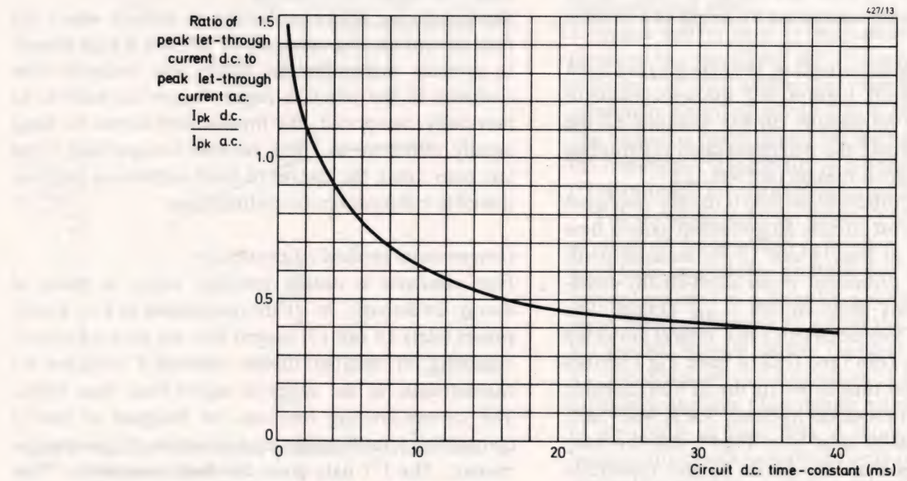


Fig.13 — Ratio of peak let-through current d.c. to peak let-through current a.c. against circuit d.c. time-constant

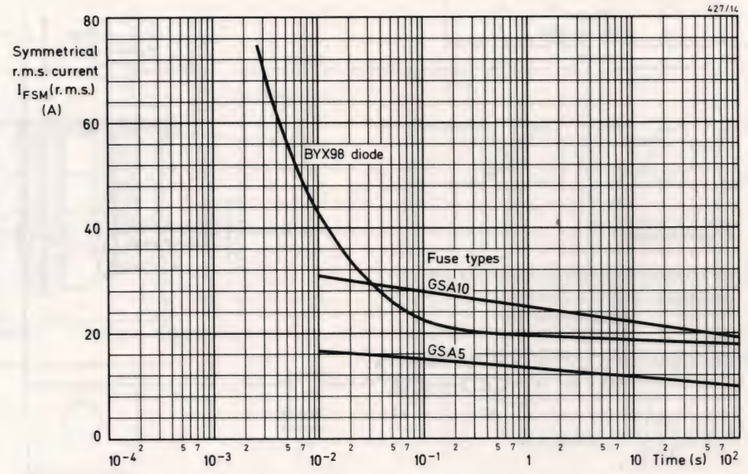


Fig.14 — Curves of surge current I_{FSM} (r.m.s.) against time for BYX98 diode protected by English Electric GSA5 and GSA10 fuses

MATCHING OF SEMICONDUCTOR DEVICES TO FUSE OPERATION

Some of the problems associated with matching semiconductor devices to fuses are considered in this section.

Overload conditions

In practical terms, the protection of diodes, thyristors, and triacs can take two principal forms:

1) Protection throughout an entire overload range up to full short-circuit conditions by means of a fuse alone;
2) Protection by means of a circuit breaker down to its minimum operating time, and for shorter periods, up to full short-circuit conditions by means of a suitable fuse.

In the second form of protection, the fuse is called upon to protect the circuit breaker and the semiconductor device. Hence the let-through current provided by the fuse should not exceed the maximum-rated interrupting capability of the circuit breaker (see Ref.12).

The fuse-only protection method is usually employed in low-power low-cost circuits. Surge current against time curves are shown in Figs.14 and 15 for semiconductor devices with fuse protection under short-circuit conditions. Fig.14 shows surge current I_{FSM} against time curves for the BYX98 diode (9A r.m.s. rating) protected by English Electric GSA5 and GSA10 fuses. Fig.15 shows surge current against time curves for the BTW24 thyristor (55A r.m.s. rating) protected by Brush 30ET, 40ET, and 55ET fuses. It will be seen from Fig.15 that the fuses have lower ratings than the device to give reasonable tracking in the overload region above one second. The problem of the low surge capability of devices to r.m.s. current in the 1s region can result in fuse-to-semiconductor-device coordination difficulties. Because of these difficulties, some restrictions may be placed on the maximum steady-state current operation of devices where fuse-only protection is used.

A more satisfactory system is to use the protection of the circuit breaker in the 1s region (see Fig.1). The circuit breaker provides 'constant current' interruption for this time region, and allows fuses of higher current rating to be used while adequate protection of the devices under short-circuit conditions is maintained.

High-current fault conditions

Semiconductor device protection in circuits where the fault current causing operation of the fuse is high enough to produce current-limiting action and complete fuse clearance in the subcycle region is now considered. As previously mentioned, the time-current curves for fuses usually terminate at 10ms, because for operating times less than 10ms the instant of fault occurrence has considerable influence on the melting time.

Conventional method of protection

Fuse clearance is usually specified solely in terms of energy let-through, or $\int i^2 dt$, rationalised to I^2t. Earlier papers (Refs.14 and 15) suggest that the forward current capability of rectifier diodes assumes a constant I^2t characteristic in the subcycle region (less than 10ms). The current-limiting fuse can be designed to have a constant I^2t let-through as a function of prospective current. The I^2t data given for fuses (see under 'Fuse curves') applies to worst-case conditions. Therefore, for most fault conditions, the I^2t let-through should be less

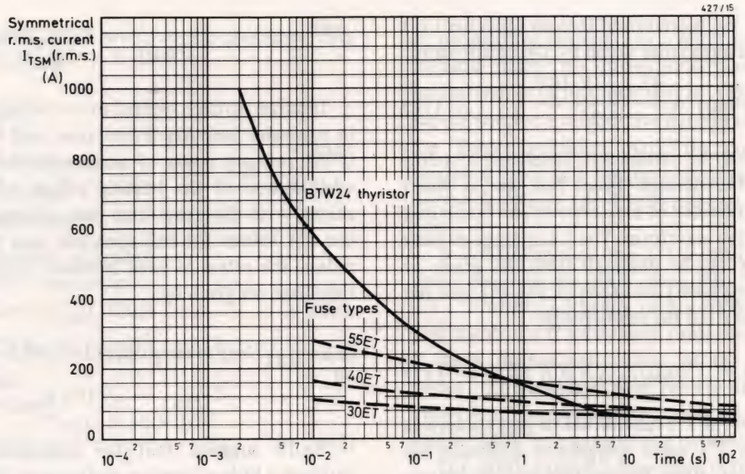


Fig.15 — Curves of surge current I_{TSM} (r.m.s.) against time for BTW24 thyristor protected by Brush 30ET, 40ET, and 55ET fuses

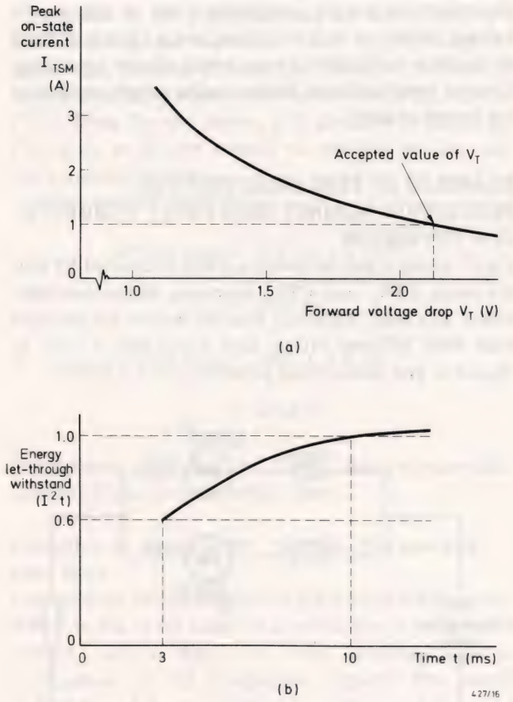


Fig.16 — Parameter limit values (indicated by broken lines) for diodes and thyristors:
(a) mean on-state current against forward voltage drop,
(b) I^2t let-through as a function of pulse width

than that shown in the published data. Conversely, the published I^2t value for the semiconductor diode, thyristor, or triac tends to be the lowest value in a complete spread of values. The probability of worst-case circuit conditions corresponding to a semiconductor device having a minimum I^2t capability is, therefore, statistically small. Based on this approach, which can be called the 'conventional' approach to fusing, a simple I^2t relationship between the fuse operating in subcycle time and the semiconductor device gives an effective method of protection in most applications.

Typical system for specifying I^2t capability of diodes, thyristors, and triacs

A typical system used by semiconductor device manufacturers for specifying the I^2t capability of a diode, thyristor, or triac enables the conventional method of protection described previously to be used with safety. The system is based largely on the method of matching the minimum I^2t capability of a device to the worst-case I^2t let-through for a nominally-rated fuse.

For any semiconductor device, it is desirable to absorb as much of the spread in parameters as possible into an acceptable marketable product. For example, V_T (d.c. forward voltage) of a thyristor is set against $I_{T(AV)}$ (the mean on-state current) to absorb the greater part of the V_T spread. Sample devices covering the full spread in V_T are subjected to a succession of 10ms half-sinewave surge-current pulses of increasing magnitude. An example of the results of these tests, in terms of I_{TSM} (thyristor non-repetitive peak on-state current) against V_T, is shown in Fig.16a in which a 'safe' contour line for pulses of 10ms period is indicated. The value of I_{TSM} for the

accepted value of V_T is converted into an equivalent I^2t value for 10ms sinewave pulse width by the relationship:

$$I^2t\,(10ms) = \frac{I^2_{TSM} \times 10^{-2}}{2}. \quad \ldots(12)$$

A further test may be carried out, consisting of a 3ms pulse applied to the devices. From this test, a direct evaluation of I^2t withstand of the device can be computed from the shape of the waveform. The r.m.s. surge current capability for 3ms can be obtained from the graph of surge current against time (for example, Fig.15), and the I^2t value computed from the relationship:

$$I^2t\,(3ms) = I^2_{TSM(rms)} \times 3 \times 10^{-3}. \quad \ldots(13)$$

A comparison of the I^2t capabilities of various devices indicates that the I^2t value sometimes decreases for periods of less than 10ms for modern encapsulations, and that the thermal processes during these short periods are not of an adiabatic nature. A curve relating the I^2t capability of a device to pulse width is shown in Fig.16b. This curve shows a decreasing value of I^2t towards the 3ms pulse-width condition.

Close coordination of fuse parameters to semiconductor device surge capability

Close coordination of fuse performance to semiconductor device performance requires knowledge of the fuse performance under particular circuit conditions. It has been stated previously that curves in fuse published data are usually given for worst-case conditions. A considerable number of tests are undertaken to determine how fuse parameters vary with circuit conditions, and the variation in three principal fuse parameters is shown in Figs.8a, 8b, and 8c.

Fig.8a indicates that the fuse peak let-through (assuming the fuse to be in the current-limiting condition) has a waveform dependent on the supply voltage. When the fuse operates under maximum-rated voltage conditions, the waveform approaches a half-sinewave shape, whereas at a low voltage, a triangular-shaped waveform is produced. The r.m.s. current for a half-sinewave pulse $I_{rms}(hs)$ is given by:

$$I_{rms}(hs) = I_{S(pk)} \Big/ \sqrt{2}, \quad \ldots(14)$$

and the r.m.s. current for a triangular-shaped pulse $I_{rms}(tr)$ is given by:

$$I_{rms}(tr) = I_{T(pk)} \Big/ \sqrt{3}. \quad \ldots(15)$$

The equivalent I^2t values are given by:

$$I^2t(hs) = \frac{I^2_{S(pk)}t}{2}, \quad \ldots(16)$$

and

$$I^2t(tr) = \frac{I^2_{T(pk)}t}{3}. \quad \ldots(17)$$

If surge current applied over a definite time, resulting in excessive junction temperature and localised melting, is the primary cause of semiconductor failure, then an examination of the heating effects of different waveshapes with the same time base is desirable. Comparing the I^2t values for half-sinewave- and triangular-shaped pulses, the ratios of peak currents for pulses of an equal time base are given by:

$$I_{T(pk)} \Big/ I_{S(pk)} = \sqrt{(3/2)},$$

or

$$I_{T(pk)} = \sqrt{(3/2)}\, I_{S(pk)}. \quad \ldots(18)$$

Eq.18 suggests that the triangular waveform will produce a higher junction temperature than the sinewave for equal I^2t values. If this is correct, then I^2t ratings for a semiconductor device based on sinewave tests may have a lower safety margin than I^2t ratings based on triangular-shaped waveform tests when the fuse clears on a triangular-shaped waveform. It will be appreciated that because the let-through current waveshape of the fuse is dependent on supply conditions (that is, the supply voltage, instant of fault condition, and p.f.), it is difficult to produce rationalised curves which closely coordinate fuses to semiconductor devices unless supply conditions are known exactly.

EXAMPLES OF FUSE SELECTION FOR PROTECTION AGAINST HIGH FAULT CURRENTS IN A THYRISTOR

Fig.17 shows a pair of inverse-parallel-connected BTW92 thyristors CSR_1 and CSR_2 supplying phase-controlled power to a load. Assuming that the devices are operated near their full-load rating, fuse 1 and fuse 2 must be chosen to give short-circuit protection of the devices.

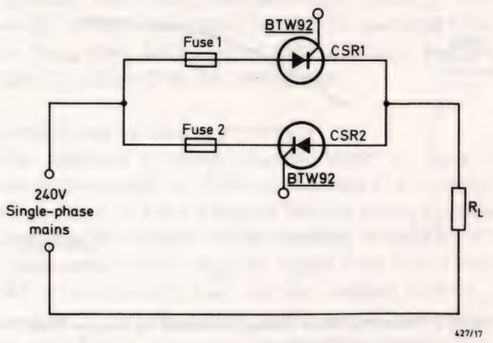


Fig.17 — Two inverse parallel connected BTW92 thyristors supplying phase-controlled power to a load

The ratings given below are from the published data for the BTW92 thyristor.

On-state conditions

Mean current $I_{T(AV)}$ = 20A

R.M.S. current $I_{T(RMS)}$ = 31A

I^2t rating (<10ms) $500A^2s$

Maximum surge current at peak of half-sinewave, and at maximum operating conditions I_{TSM}(10ms) = 320A

The I^2t value is derived directly from the I_{TSM} value by the relationship:

$$I^2t = \frac{I^2_{TSM} \times 10 \times 10^{-3}}{2}, \quad \ldots(19)$$

or

$$I^2t = \tfrac{1}{2}(320^2 \times 10 \times 10^{-3}),$$

$$= 512A^2s.$$

Included in the published data for the BTW92 is a graph showing the maximum r.m.s. surge current (A) against the duration of surge (s). The curve is based on sinewave pulses applied to the device. Given the value of I^2t at 10ms for the device, it is advisable to check the I^2t values at shorter periods to establish the law that this parameter follows.

From the published data:

$$I^2t \text{ for } 5ms = 315^2 \times 5 \times 10^{-3},$$

$$\simeq 500A^2s;$$

$$I^2t \text{ for } 4ms = 360^2 \times 4 \times 10^{-3},$$

$$\simeq 520A^2s.$$

These values show that the BTW92 has a substantially constant I^2t let-through below 10ms.

Protection by Ferraz 600V, type RE, 25A and 32A rated fuses

Examples of curves for Ferraz 600V type RE fuses are shown in Fig.7c for total I^2t as a function of prospective current, and in Fig.9 for total operating time as a function of the prospective current. The curves in Figs.7c and 9 are expressed in multiples of the rated current. Where the device is to be used at full-load current, fuses rated at 25A or 32A can be considered. By examining the curves shown in Fig.7c, it will be seen that the I^2t let-through decreases slightly at the higher values of prospective current. For a 600V type RE fuse of 25A nominal rating, the curves show that the maximum I^2t let-through is ($650A^2s \times 0{\cdot}5$) or $325A^2s$ for a 240V a.c. supply and for a prospective current of 500A r.m.s. From the Ferraz published data, the curves showing fuse clearance time as a function of prospective current and operating voltage (see Fig.9) indicate a clearance time of 5ms.

A comparison of the I^2t let-through and clearance time ratings of the 600V, type RE, 25A rated fuse and the I^2t withstand rating of the BTW92 thyristor shows that the device is adequately protected.

As a further verification of the protection of the device, the published data for the 600V type RE fuses shows that the peak let-through current of the 25A rated fuse is 500A for a prospective current of 500A r.m.s.

The 600V type RE fuse has a 600V r.m.s. rating, and the fusing current against time can be assumed to have a triangular waveform. The equivalent I^2t let-through for the fuse calculated from the peak current will be:

$$\frac{500^2 \times 5 \times 10^{-3}}{3} = 417A^2s. \quad \ldots(20)$$

The maximum on-state peak surge current for the BTW92 is given in the published data as 320A for 10ms, and 447A for 5ms.

In the section 'Matching of semiconductor devices to fuse operation', it is shown (Eq.18) that for equal time base and I^2t values, the relationship between I_{pk} for a triangular wave to I_{pk} for a sinewave is $\sqrt{(3/2)}$. Therefore, a 320A peak sinewave pulse can be equated to $320\sqrt{(3/2)}$ or 392A for a peak triangular pulse.

The above verification indicates that the BTW92 is adequately protected by the 600V, type RE, 25A rated fuse at the value of prospective current chosen. Similarly, for higher values of prospective current for a fuse of the same type and rating, the calculations below are made for the BTW92.

1) Fuse I^2t let-through current at 2500A r.m.s. prospective current

$$= 590 \times 0{\cdot}5,$$

$$= 295A^2s.$$

2) Fuse clearing time = 1·5ms.

3) Thyristor non-repetitive peak current I_{TSM} for 1·5ms sinusoidal pulse (assuming a constant I^2t value for the device)

$$= \sqrt{\left[(2 \times 500) \Big/ (1{\cdot}5 \times 10^{-3})\right]},$$

$$= 816A.$$

4) Fuse peak current (I_{pk}) = 890A.

5) Fuse I^2t let-through calculated from peak current I_{pk} (assuming fusing current has a triangular waveform)

$$= \tfrac{1}{3}\,(890^2 \times 1{\cdot}5 \times 10^{-3}),$$

$$= 396A^2s.$$

6) Fuse peak current (calculated from peak sinusoidal current of device, assuming I^2t values for device and fuse are equal)

$$= 816\sqrt{(3/2)},$$

$$= 1000A.$$

Calculations 1 to 6 indicate an adequate safety margin for the thyristor protected by the fuse.

The performance of the 600V, type RE, 32A rated fuse is considered in a similar manner. The BTW92 is the device protected by the fuse.

1) Fuse I^2t let-through current at 500A r.m.s. prospective current

$$= 1000 \times 0{\cdot}5,$$

$$= 500A^2s.$$

2) Fuse clearing time = 6ms.

3) Thyristor non-repetitive peak current I_{TSM} for 6ms sinusoidal pulse (assuming a constant I^2t value for the device)

$$= \sqrt{[(2 \times 500)/(6 \times 10^{-3})]},$$

$$= 408A.$$

4) Fuse peak current (I_{pk}) = 580A.

5) Fuse I^2t let-through calculated from peak current I_{pk} (assuming fusing current has a triangular waveform)

$$= \tfrac{1}{3}\,(580^2 \times 6 \times 10^{-3}),$$

$$= 673A^2s.$$

6) Fuse peak current (calculated from peak sinusoidal current of device, assuming I^2t values of device and fuse are equal)

$$= 408\sqrt{(3/2)},$$

$$= 500A.$$

The calculations are repeated for the higher value of prospective current.

1) Fuse I^2t let-through current at 2500A r.m.s. prospective current

$$= 920 \times 0{\cdot}5,$$

$$= 460A^2s.$$

2) Fuse clearing time = 1·8ms.

3) Thyristor non-repetitive peak current I_{TSM} for 1·8ms sinusoidal pulse (assuming a constant I^2t value for the device)

$$= \sqrt{[(2 \times 500)/(1{\cdot}8 \times 10^{-3})]},$$

$$= 745A.$$

4) Fuse peak current (I_{pk}) = 1000A.

5) Fuse I^2t let-through calculated from peak current I_{pk} (assuming fusing current has a triangular waveform)

$$= \tfrac{1}{3}\,(1000^2 \times 1{\cdot}8 \times 10^{-3}),$$

$$= 600A^2s.$$

6) Fuse peak current (calculated from peak sinusoidal current of device, assuming I^2t values of device and fuse are equal)

$$= 745\sqrt{(3/2)},$$

$$= 912A.$$

The calculations indicate that the Ferraz 600V, type RE, 25A rated fuse will fully protect the BTW92 over a wide range of prospective supply current. The 600V, type RE, 32A rated fuse provides a narrower safety margin at low prospective currents.

Protection by English Electric type GSA25 25A rated fuse

Fig.18a shows the cut-off current characteristics, and Fig.18b shows the I^2t variation with prospective current, for English Electric type GSA fuses at 240V r.m.s. The I^2t let-through of the GSA25 fuse increases as a function of the prospective current of the supply. This increasing I^2t value sets a limit on the prospective current capability of the mains supply. No data is provided on the clearing time of the GSA25, although a reasonably accurate value can be calculated from the fuse published data available.

The parameters below apply to the GSA25 and the BTW92.

1) Thyristor I^2t rating = $500A^2s$
2) For the 25A rated fuse to carry $500A^2s$ let-through, the prospective current is limited to 15kA r.m.s. or 21kA peak
3) Fuse peak current let-through (I_{pk}) (from fuse curves) = 1300A
4) Fuse pre-arc or melting I^2t let-through K = $80A^2s$

The fuse clearing time is calculated below (see also under 'Fuse operation').

From Eq.11, fuse melting I^2t is given by:

$$K = \int_0^t i^2_m \, dt_m. \qquad \ldots(21)$$

The maximum rate of rise of current (di/dt) and peak melting current occur in a symmetrical fault period. Therefore:

$$di/dt = \omega I_{pk}(sym), \qquad \ldots(22)$$

and

$$i_m = \omega I_{pk}(sym)\, t_m, \qquad \ldots(23)$$

where i_m is the instantaneous current when the fuse element melts, and t_m is the melting time.

Eq.21 becomes:

$$K = \int_0^{t_m} \left(\omega^2 I^2_{pk}\,(sym)\, t^2_m\right) dt_m,$$

$$= \tfrac{1}{3}\,(\omega^2 I^2_{pk}\,(sym)\, t^3_m),$$

$$= \tfrac{1}{3}\,(di/dt)^2\, t^3_m. \qquad \ldots(24)$$

The current waveform in Fig.19 shows the clearing time for the GSA25, and the shaded area represents the I^2t melting value K. Therefore:

$$K = \frac{I^2_{pk(m)} t_m}{3}.$$

also:

$$K = \frac{(di/dt)^2\, t^3_m \times 10^{12}}{3},$$

or

$$3K = t^3_m\,(di/dt)^2 \times 10^{12}, \qquad \ldots(25)$$

where di/dt is expressed in A/μs.

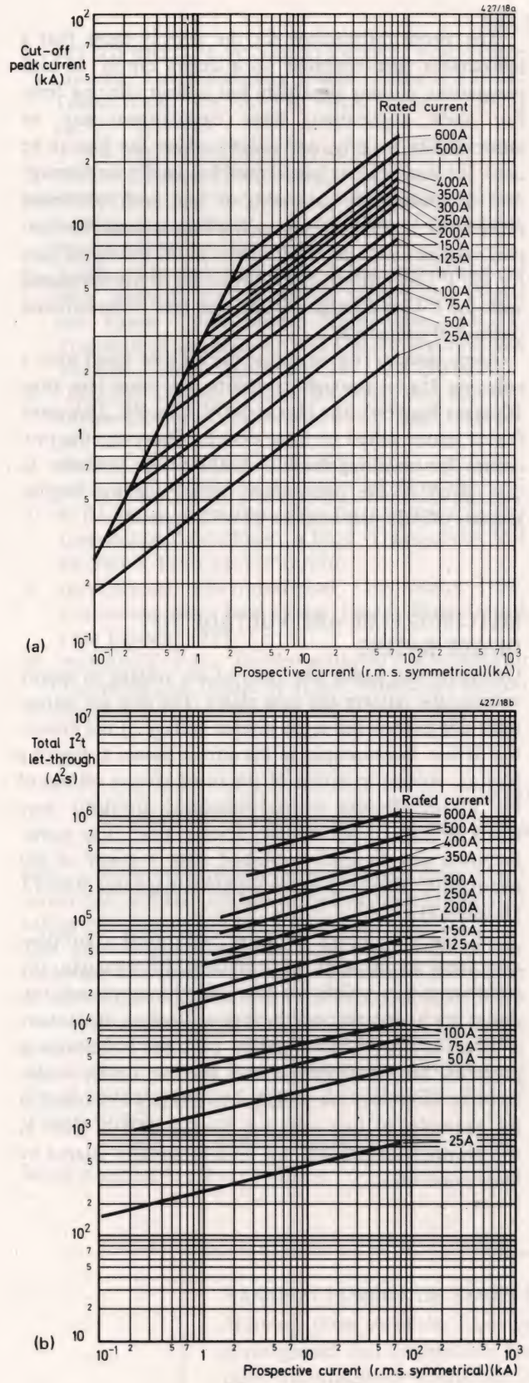


Fig.18 – English Electric fuses, type GSA, at 240V r.m.s.:
(a) cut-off current characteristics,
(b) I^2t variation with prospective current

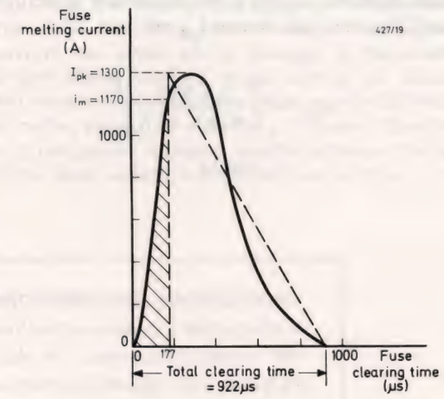


Fig.19 – Melting current against clearing time for English Electric type GSA25 fuse rated 25A. The shaded area represents the I^2t (melting) let-through K

From Eq.25, t_m is given by:

$$t_m = \left[\frac{3K \times 10^{-12}}{(di/dt)^2}\right]^{1/3}. \quad \ldots(26)$$

From parameter 2 and Eq.22:

$$di/dt = 314 \times 21 \times 10^3 \times 10^{-6},$$
$$= 6{\cdot}6A/\mu s.$$

Therefore:

$$t_m = \left[\frac{3 \times 80 \times 10^{-12}}{6{\cdot}6^2}\right]^{1/3},$$
$$= 177\mu s;$$

and:

$$i_{m(pk)} = [3K\, di/dt]^{1/3},$$
$$= [3 \times 80 \times 6{\cdot}6 \times 10^6]^{1/3},$$
$$= 1170A.$$

The total I^2t let-through of the fuse (from parameter 2) is $500A^2s$; therefore the I^2t arcing let-through is $420A^2s$. Therefore arcing time t_{arc} is given by:

$$t_{arc} = \frac{3 \times 420}{1300^2},$$
$$= 745\mu s.$$

The total clearing time for the fuse is approximately $920\mu s$ as shown in Fig.19. For a sinewave pulse of time base $920\mu s$, the peak current I_{pk} will be:

$$I_{pk} = \left[\frac{2 \times 500}{920 \times 10^{-6}}\right]^{1/2},$$
$$= 1042A.$$

The above calculations for the GSA25 show that a low-current fuse operated on a mains supply of high prospective current capability has a short clearing time. For many applications these calculations may be unnecessarily lengthy, particularly where the fuse to be used for short-circuit protection has an I^2t let-through that is substantially constant, or falls with increasing prospective current. Where such a fuse is used, the user may consider only the values given in the published data for the I^2t let-through of the protected device compared with the I^2t let-through for the fuse (see 'Conventional method of protection').

Some devices (for example, the BTX94 triac) have a reducing I^2t let-through capability for times less than $10\mu s$ (see Fig.16b). The Ferraz 600V, type RE, 25A rated fuse is better suited to these devices. However, the procedure for matching the fuse to the device is similar to that given in the calculations above for the English Electric GSA25 fuse and the BTW92 thyristor.

MATCHING FUSE ARC VOLTAGE TO DEVICE RATING

Generally, the higher the ratio of arc voltage to supply voltage, the quicker the fuse clears. The fuse arc voltage must not exceed the rated inverse voltage of the protected device. For example, in the circuit shown in Fig.17 a fuse arc voltage in excess of the rated inverse voltage of the non-conducting parallel-connected thyristor may result in breakdown of the device. Most fuse manufacturers give in their published data a graph of the relationship of arc voltage to supply voltage (see Refs.13, 16, and 17).

In practical fusing problems, additional conditions may need to be taken into account, for example, the environment in which the fuse and the semiconductor device are to operate, and the type of load on the system. A large amount of information on these conditions is given by the fuse manufacturer and the device manufacturer. However, the principal techniques embodied in the examples of fuse selection for the BTW92 given in the previous section will not be substantially altered by these conditions.

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APPENDIX 1

Triggering a Thyristor or Triac which has a Short-circuit Load

When a thyristor or triac is triggered under normal load conditions, a finite current-spreading time is required before full conduction at rated current can take place. This current-spreading time is usually given in the published data for the device as a permissible rate of rise of current (di/dt) in the device in terms of $A/\mu s$. When the source impedance is the impedance of an a.c. power line, Fig.3 shows that when θ is equal to 0° the initial rate of rise of current is zero, and the maximum rate of rise of current will occur when θ is equal to $\pi/2$. When θ is equal to $\pi/2$:

$$di/dt = E_{pk}/L,$$

which is similar to a d.c. condition.

As the p.f. of the source increases towards unity, the value of di/dt when θ is equal to 90° increases to the limiting condition $L \rightarrow 0$ and $di/dt \rightarrow \infty$. It will be seen that if a thyristor or triac is triggered into a short-circuit condition when supplied from a largely-resistive source of an a.c. or d.c. system, then a fuse cannot protect the device from the initial rate of rise of surge current. Therefore, the device will be damaged. In this article it has been shown that a.c. power sources are inductive under short-circuit conditions. With the typical inductance values associated with the a.c. system, the rate of rise of prospective current is usually moderate compared with the di/dt capability of the thyristor or triac.

MANUFACTURERS OF FUSES FOR SEMICONDUCTOR PROTECTION

Although three particular fuse manufacturers are mentioned in this article, it is recognised that comparable fuses are made by other manufacturers. The three manufacturers mentioned have been selected because their fuses are typical of most semiconductor protection fuses.

No preference is intended by inclusion in or omission from this present article.

Product Information:

Gapped Ferroxcube E-cores for switched-mode power supplies

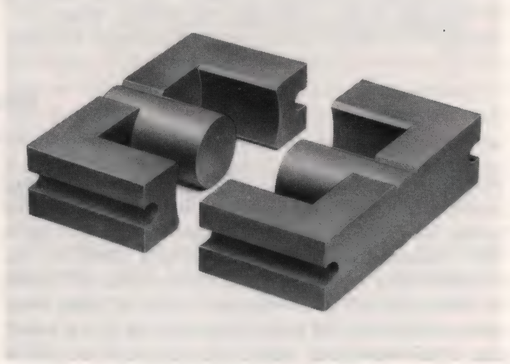
The well-established FX3700 series of cores has found wide application in output transformers for push-pull and forward converters in switched-mode power supplies. Now, each core in the series has been supplemented by one with a gap ground in the centre pole. The gaps are dimensioned so that pairs of cores can be used for smoothing chokes at the outputs of SMPSs. Equally, the cores are suitable for use in the output transformers of SMPSs using flyback converters.

MECHANICAL AND ELECTRICAL DATA

The fundamental data for these cores is identical to that of the basic cores from which they are derived, as follows:

FX3721 is derived from FX3720 (and uses DT2720 coil former),
FX3731 is derived from FX3730 (and uses DT2730 coil former),
FX3741 is derived from FX3740 (and uses DT2740 coil former),
FX3751 is derived from FX3750 (and uses DT2750 coil former).

The saturation flux characteristics are still valid, except that higher values of magnetising ampere-turns (NI) are necessary to achieve saturation. The graphs for core loss as a function of total flux, and typical temperature rise as a function of total transformer loss, are also still applicable. A brief extract of data for the new gapped cores is given in Table 1. The latest data on these types should be consulted during circuit design work.



A pair of E-cores for SMPSs showing gap in centre pole

TABLE 1 Tentative Data

Parameter	FX3721	FX3731	FX3741	FX3751
Air gap length, l_g (mm)	1·2 to 1·6	1·3 to 1·7	2·1 to 2·5	4·65 to 5·05
Maximum magnetising ampere-turns at 100°C, NI (amperes)	305	350	525	875
A_L value for a pair of cores (nH/turn^2),				
max.	69	90	90	77
min.	57	78	80	72

Power-handling capability of ferrite transformers and chokes

for switched-mode power supplies

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UDC 621.3.016.2: 621.314.2: 621.318.42: 621.318.132: 621.311.68

A single equation is evolved for the power-handling capability of nine classes of transformer and two classes of choke used in fixed-frequency push-pull forward and flyback converters in switched-mode power supplies (SMPS). The equation consists of three principal terms. The first term describes the winding and the permissible dissipation in the winding for a given overall temperature rise. The second term is the product of frequency and peak flux under steady-state operating conditions. The third term is a number which is tabulated for the classes of transformer and choke. The equation is applicable to power supplies in which the output voltage is held constant by a feedback loop which controls the duty cycle of the output switching stage. Additional equations are given for the output current range for good regulation, and for the required turns-per-volt. An example of the use of the equations is included.

INTRODUCTION

Three types of converter are used in switched-mode power supplies: the flyback converter, the forward converter, or the push-pull converter (see Ref.1). The principal wound component in each type of converter is the output transformer. An output choke is used in addition to the output transformer in the forward converter and the push-pull converter. The power-handling capability of these wound components is governed by the factors given below:

1) the geometry of the core and the windings;
2) the permitted temperature rise;
3) the operating frequency;
4) the ratio of minimum to maximum supply voltage;
5) the ratio of minimum to maximum load current over which good output voltage regulation is required, and over which the duty cycle remains approximately constant for a fixed input voltage (Ref.2);
6) the percentage of the 'window' area occupied by copper;
7) the a.c.-to-d.c. resistance ratio of the windings (Refs.3, 4, and 5);
8) the peak flux density in the core under steady-state operating conditions.

When a core is considered for a given application, factors 1 to 5 will be known, and practical values can be assigned to factors 6 and 7.

Factor 8 is generally chosen so that under transient conditions, when a load is suddenly applied at the power supply output, and maximum duty cycle occurs together with maximum supply voltage, core saturation is just avoided when the core is operating at a chosen maximum temperature. The ratio of maximum permissible peak

flux density to steady-state peak flux density then equals the ratio of maximum d.c. supply voltage to minimum d.c. supply voltage (factor 4), modified sometimes for forward converters by a small allowance for the remanent flux in the core.

Push-pull transformers may be subject to an allowance for flux 'staircasing' due to imperfect balance in the circuit, and to an allowance for flux-doubling due to sudden changes from minimum to maximum duty cycle accompanying, for example, a sudden change from minimum to maximum load current. Automatic balancing and slow ramp-up circuitry can minimise these effects, and a fast-acting current limit can in some circumstances protect the transistors in the event of transient excursions into core saturation. The appropriate safety factor therefore depends on the circuit design.

In addition, for maximum efficiency of the transformer, the working flux density must be limited to a value where the core loss does not exceed a given fraction (about a half) of the allowable dissipation. The precise value of this fraction depends on the loss characteristic of the core.

In this article, an equation is derived for the power-handling capability of eleven classes of transformer and choke. The equation relates power-handling capability to the permissible power loss in the windings, which for a given temperature rise can be determined from the total permissible dissipation and the core loss.

The results are summarised in the section 'Summary of Equations' using symbols defined in the section 'Symbols and definitions'. In Appendix 1, the relationship between ampere-turns and power loss in the windings is deduced, and this relationship is used in Appendices 2 to 5 where the power-handling capability of each class of transformer or choke is calculated.

Turns ratios of 1:1 are assumed in all transformer calculations because practical turns ratios do not affect the power-handling capability of transformers, provided that the required packing factors and a.c.-to-d.c. resistance ratios are achieved in practice.

Because efficiencies in the region of 97% are typical for most components considered here, and to simplify the equations, output power is calculated as being equal to input power without subtraction of losses.

SYMBOLS AND DEFINITIONS

The symbols defined below are those used in the calculations throughout this article, and are given in SI units.

Symbol	*Definition*
A_e	Effective area of magnetic path
A_w	Cross-sectional winding area within the coil former
B_e	Effective flux density
C_1	Core factor $C_1 = \ell_e/A_e$
f	Operating frequency of converter
F_R	$\frac{\text{A.C. resistance of winding}}{\text{D.C. resistance of winding}}$
F_w	Winding copper factor: $= \frac{\text{total cross-sectional area of copper in winding}}{A_w}$
I, I_{dc}, I_idc, I_odc, I_p, I_s	Currents as indicated in diagrams
I_{mag}	Magnetising current
I_o	D.C. output current
I_omin	Minimum value of I_o for good regulation
I_omin_{ch}	Component of I_omin attributable to choke
I_omin_{tr}	Component of I_omin attributable to transformer
I_{rms}	R.M.S. current flowing in utilised windings
K	Arbitrary constant used in Appendix 4 (Eq.54)
K_1	Arbitrary constant used in Table 1 (Eq.13)
K_2	Arbitrary constant used in Appendix 6 (Eq.93)
K_3, K_4	Arbitrary constants used in Appendix 8 (Eq.100)
ℓ_e	Effective length of magnetic path
l_w	Mean turn length of windings
m	Multiplying factor for ρ_c to obtain resistivity at elevated temperature
n	Steinmetz exponent
N_p	Number of primary turns
N_s	Number of secondary turns
N_t	Total number of turns in windings
N_u	Total number of turns in the utilised windings
P_c	Power loss in the core
$Pmin_{ch}$	$Pmin_{ch} = \Delta_{ch}P_o$, where P_o is the power-handling capability of the choke (For push-pull converters *only*, Pmin = $Pmin_{tr}$ + $Pmin_{ch}$ for the complete power supply)
$Pmin_{tr}$	$Pmin_{tr} = \Delta_{tr}P_o$, where P_o is the power-handling capability of the transformer
P_o	Power-handling capability of a transformer with duty cycle δ = 0·5, or of a choke over a given input voltage range
P_o'	Power-handling capability of a transformer with a given value of δ
P_t	Total loss in transformer: $P_t = P_w + P_c$
P_w	Permissible total power loss in windings for a given temperature rise
R_t	Total effective resistance of all windings
R_u	Total effective resistance of the utilised windings

Symbol	*Definition*
SF	Safety factor by which $\hat{\Phi}$ is divided to allow for flux imbalance in push-pull transformers
T	Cycle time
T_{amb}	Local ambient temperature
T_{max}	Maximum 'hot-spot' temperature
T_{rise}	Ambient to 'hot-spot' temperature rise
U_F	Winding utilisation factor. (U_F = 1 for a two-winding transformer, or $\frac{2}{3}$ for a transformer with an energy recovery winding carrying negligible current and occupying $\frac{1}{3}$ of the winding space)
V, V_{dc}, V_idc, V_odc, V_p, V_s	Voltages as indicated in diagrams
V_e	Effective magnetic volume
V_i	D.C. input voltage
V_imax	Maximum d.c. input voltage
V_imin	Minimum d.c. input voltage
V_o	D.C. output voltage
X, Y, Z	Arbitrary symbols for terms used in Eq.1
a	V_imax/V_imin
Δ	Minimum d.c. output current for good regulation / Maximum d.c. output current
Δ_{ch}	Value of Δ for a choke
Δ_{tr}	Value of Δ for a transformer
δ	Duty cycle of transistor collector current, or of choke input voltage as used in Appendix 5
μ_a	Relative amplitude permeability
μ_o	$4\pi \times 10^{-7}$ H/m
ρ_c	Resistivity of copper at 20°C
$\hat{\Phi}$	Peak flux in the core under steady-state operating conditions (less remanent flux where applicable)
$\hat{\Phi}max$	Maximum peak flux to avoid saturation

SUMMARY OF EQUATIONS

The derivation of all the equations presented in this section is given in Appendices 1 to 7.

Maximum power-handling capability

The maximum power-handling capability of a transformer or choke is given by:

$$\boxed{P_o = XYZ} \quad . \qquad \ldots(1)$$

The terms X, Y, and Z are arbitrary symbols, where:

$$X = \left[\frac{P_w A_w F_w}{\rho_c m l_w F_R}\right]^{1/2}, \qquad \ldots(2)$$

$$Y = \hat{\Phi} f, \qquad \ldots(3)$$

and

Z is a number.

The number Z has a different value for each class of transformer or choke.

For push-pull and forward converter transformers, the values of Z are simple numbers given in Table 1. For flyback converter transformers and chokes, the values of Z can be calculated from the subsidiary equations also given in Table 1.

Volts-per-turn

The volts-per-turn required to obtain the value of P_o shown in Eq.1 are given by:

volts-per-turn $= 4f\hat{\Phi}$, $\ldots(14)$
for push-pull converter transformers;

volts-per-turn $= 2f\hat{\Phi}$, $\ldots(15)$
for forward converter transformers;

volts-per-turn $= 4f\hat{\Phi}\dfrac{\Delta}{1+\Delta}$, $\ldots(16)$
for flyback converter transformers.

(Note that the values are calculated at minimum supply voltage, when δ is 0·5.)

Minimum output power Pmin

For all the wound components considered in this article, except the ringing-choke transformer, there is a range of output current between the maximum value (limited by temperature rise) and a minimum value, over which the d.c. output voltage stays approximately constant if the input voltage and the duty cycle also remain constant. Below the minimum or 'boundary' value of output current, the output voltage rises rapidly because the d.c. load current is insufficient to absorb the magnetising current in the transformer or choke. To compensate for this increase in output voltage, the power supply feedback loop must operate rapidly to reduce the duty cycle, resulting in impaired regulation. The minimum power output Pmin corresponds to the boundary current value, and is given below for transformers and chokes in SMPS converters, using the relationship:

$$\Delta = \text{Pmin}/P_o.$$

Push-pull converter transformers

For push-pull converter transformers, the term Δ does not appear in the equation for P_o, but Δ_{tr} can be calculated.

From Appendix 7, Δ_{tr} is given as:

$$\Delta_{tr} = \frac{\hat{\Phi}}{XZ} \cdot \frac{\ell_e}{A_e} \cdot \frac{1}{\mu_a} \cdot \frac{10^7}{\pi}, \qquad \ldots(17)$$

where X and Z are the values used in the calculation of P_o.

Alternatively, from Appendix 7, Pmin_{tr} is given by:

$$\text{Pmin}_{tr} = \hat{\Phi}^2 \cdot \frac{\ell_e}{A_e} \cdot \frac{f}{\mu_a} \cdot \frac{10^7}{\pi}. \qquad \ldots(18)$$

Forward converter transformers

In forward converters, the transformer magnetising current is not part of the output current, and so:

$$\Delta_{tr} = 0,$$

and

$$\text{Pmin}_{tr} = 0.$$

Flyback converter transformers

In flyback converter transformers, the value of P_o depends on Δ_{tr} as shown in Eqs.9 and 11. The desired minimum-to-maximum load-current ratio Δ_{tr} must therefore be specified before P_o can be calculated.

Chokes

In push-pull converters, the minimum output current (or power) for good regulation depends on the transformer and the choke. Where a push-pull converter is used in an SMPS, Pmin for the complete power supply is (Pmin_{tr} + Pmin_{ch}). In forward converters, Pmin_{tr} is zero, and thus Pmin for the complete power supply is Pmin_{ch}.

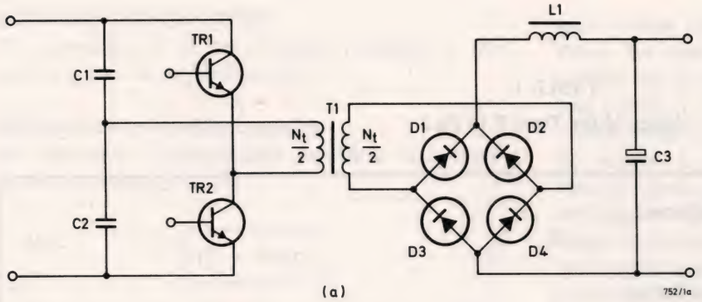
Because Eq.13 includes Δ, the value of this term must be specified before the value of P_o for the choke can be calculated.

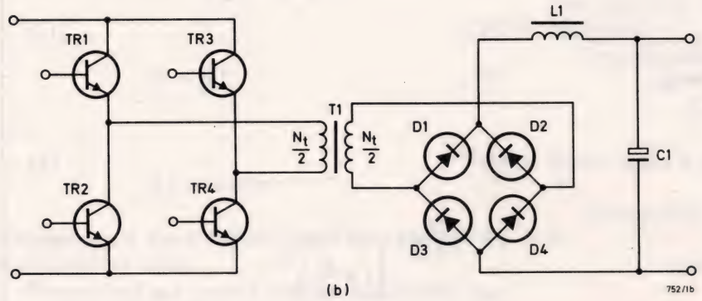
TABLE 1

Values of the Term Z in Eq.1

Two-winding push-pull converter transformer (see Figs.1a and 1b)	$Z = 2$	$\ldots(4)$
Three-winding push-pull converter transformer (see Figs.1c, 1d, and 1e)	$Z = 2\sqrt{(2/3)}$	$\ldots(5)$
Four-winding push-pull converter transformer (see Fig.1f)	$Z = \sqrt{2}$	$\ldots(6)$
Forward converter transformer (see Fig.2a)	$Z = 1/\sqrt{2}$	$\ldots(7)$
Forward converter transformer with energy recovery winding occupying $\frac{1}{3}$ of the winding space (see Fig.2b)	$Z = 1/\sqrt{3}$	$\ldots(8)$
Flyback converter transformer (see Fig.2c)	$Z = \sqrt{2} \cdot \dfrac{\Delta}{1+\Delta} \cdot \dfrac{1}{\left[1+\frac{\Delta^2}{3}\right]^{1/2}}$	$\ldots(9)$
Ringing-choke transformer* (see Fig.2c)	$Z = \frac{1}{2}\sqrt{(3/2)}$	$\ldots(10)$
Flyback converter transformer with voltage-limiting winding occupying $\frac{1}{3}$ of the winding space (see Fig.2d)	$Z = 2/\sqrt{3} \cdot \dfrac{\Delta}{1+\Delta} \cdot \dfrac{1}{\left[1+\frac{\Delta^2}{3}\right]^{1/2}}$	$\ldots(11)$
Ringing-choke transformer* with voltage-limiting winding occupying $\frac{1}{3}$ of the winding space (see Fig.2d)	$Z = \frac{1}{2}$	$\ldots(12)$
Choke	$Z = 4 \cdot \dfrac{\Delta}{1+\Delta} \cdot \dfrac{1}{\left[1+\frac{\Delta^2}{3}\right]^{1/2}} \cdot \dfrac{1}{\left(K_1 - \frac{V_i \text{min}}{V_i \text{max}}\right)}$, where $K_1 = 1$ for choke in push-pull converter (shown in Figs.1a to 1f), and $K_1 = 2$ for choke in forward converter (shown in Figs.2a and 2b).	$\ldots(13)$

*The ringing-choke converter transformer is a flyback converter transformer with $\Delta = 1$





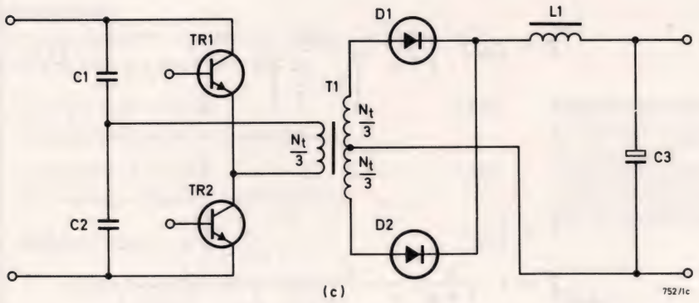
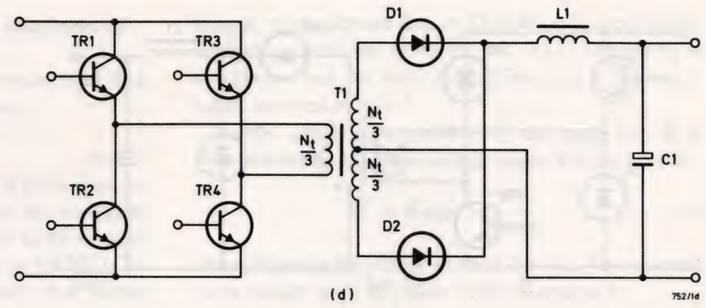
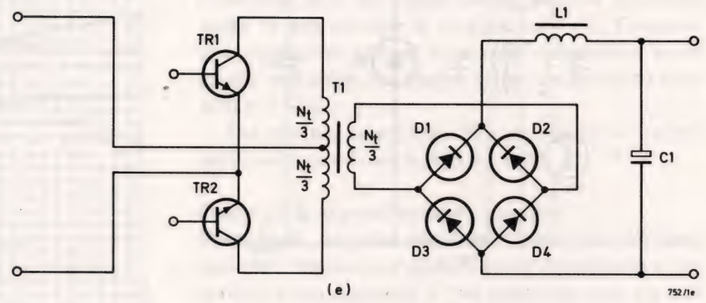
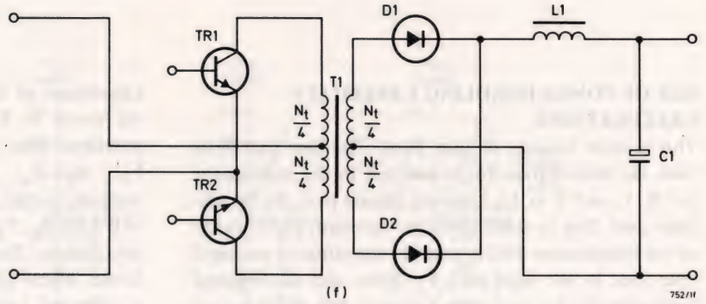


Fig.1 — SMPS converters using two-, three-, and four-winding transformers:
(a) two-winding transformer in single-ended push-pull converter with bridge-rectified output,
(b) two-winding transformer in bridge converter with bridge-rectified output,
(c) three-winding transformer in single-ended push-pull converter with bi-phase output,







(d) three-winding transformer in bridge converter with bi-phase output,
(e) three-winding transformer in push-pull converter with bridge-rectified output,
(f) four-winding transformer in push-pull converter with bi-phase output

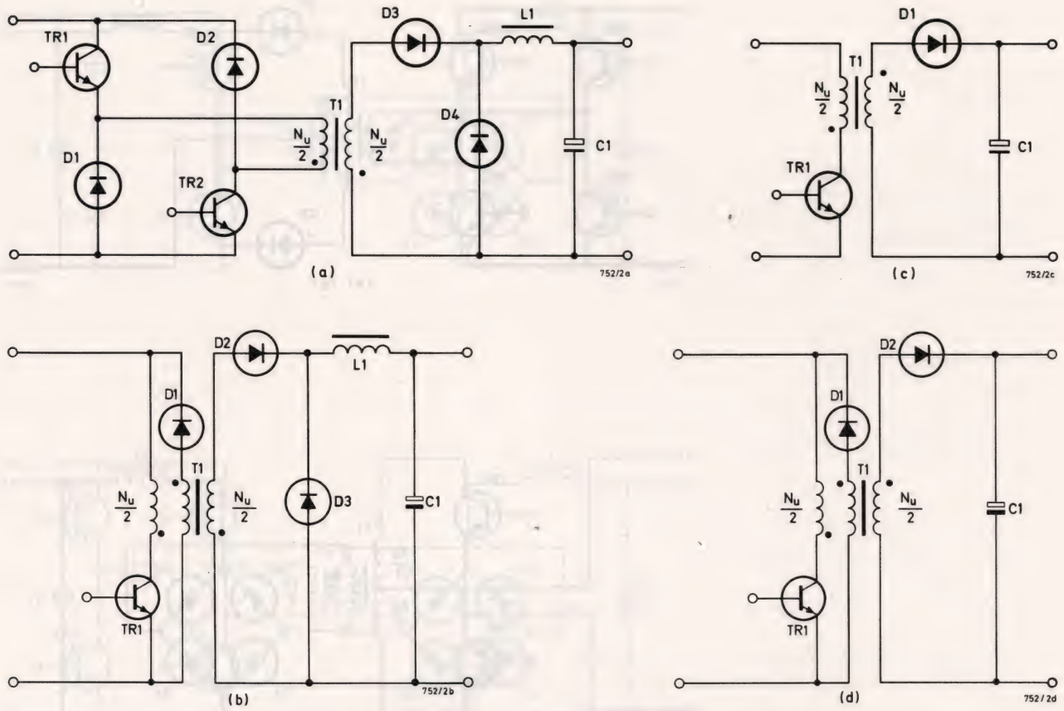


Fig.2 – Forward and flyback converters using two- and three-winding transformers:
(a) two-winding transformer in forward converter,
(b) three-winding transformer in forward converter,
(c) two-winding transformer in flyback converter,
(d) three-winding transformer in flyback converter

USE OF POWER-HANDLING CAPABILITY CALCULATIONS

This section consists of four parts. The first part deals with the information to be inserted in the expressions for X, Y, and Z in Eq.1. In the second part, the steady-state peak flux is determined for optimum performance of the transformer; that is, to avoid saturation or excessive core loss. In the third part, P_o, Pmin, and the required turns-per-volt for push-pull, forward, and flyback converter transformers is calculated. The fourth part is headed 'Notes on accuracy of calculations', and gives practical guidance on the application of the power-handling calculations and associated calculations to practical transformer designs.

The Mullard FX3730 Ferroxcube E-core is used as a practical example in this section. A converter operating frequency of 25kHz will be assumed in the calculations.

Calculation of X, Y, and Z

All terms in Eq.2 for X can be obtained from the published data for the core, with the exception of F_w, F_R, and P_w. Before the transformer windings are designed, terms F_w and F_R will not be known. A value of 0·4 for F_w/F_R will therefore be assumed in subsequent calculations. The value of 0·4 would apply to a transformer where 50% of the winding area within the former is occupied by copper, giving a value for F_w of 0·5, together with a value for F_R of 1·25. These values are typical for well-designed windings (see Refs.3 and 5 for further information on winding design).

The value of Z for the different classes of transformer and choke are given in Table 1, and since the frequency of 25kHz has been assumed, only the steady-state peak flux $\hat{\Phi}$ in Eq.3 for Y and the value of P_w in Eq.2 for X remain to be assessed. After $\hat{\Phi}$ has been obtained, the value of P_w can be calculated, as will be shown.

Choice of steady-state peak flux $\hat{\Phi}$ and assessment of core loss P_c and winding loss P_w

This part deals with the choice of steady-state peak flux $\hat{\Phi}$ to avoid saturation or excessive core loss.

Choice of $\hat{\Phi}$ to avoid core saturation

Typical magnetisation curves for the FX3730 core are shown in Fig.3. These curves show that the maximum peak flux $\hat{\Phi}$max must be restricted to 32·2μWb to avoid saturation, assuming a core temperature of 100°C. In an SMPS, with overall feedback to control the output voltage, this maximum flux of 32·2μWb may occur under transient conditions when the d.c. input voltage V_i is maximum, and the duty cycle δ also has a maximum value, assumed to be 0·5.

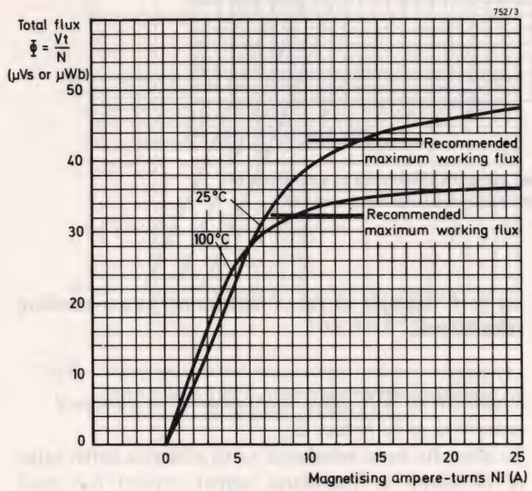


Fig.3 – Typical magnetisation curves for a pair of FX3730 cores

Under steady-state conditions, the peak flux $\hat{\Phi}$ is constant within the input voltage range, and has a value:

$$\hat{\Phi} = \hat{\Phi}\text{max} \cdot \frac{V_i\text{min}}{V_i\text{max}}, \qquad \ldots(19)$$

where $V_i$min is the voltage at which δ = 0·5. For example, for a voltage range of 230 to 370V, $\hat{\Phi}$ is given by:

$$\hat{\Phi} = 32{\cdot}2 \times \frac{230}{370},$$

$$= 20\mu\text{Wb}.$$

(Note that only the supply voltage *range* is important, which in this example is 370/230, or 1·61. Therefore, this calculation and all subsequent calculations could equally well apply to a battery whose voltage varies from 10·0 to 16·1V.)

The resulting steady-state flux excursions for various applications are shown in Figs.4a to 4d.

Choice of $\hat{\Phi}$ to avoid excessive core loss

From Fig.5, the total transformer loss P_t is 2·6W for a 'hot-spot' temperature 40degC above the ambient temperature. From Appendix 8, the maximum value for core loss is given by:

$$P_c = \frac{P_t}{1 + \frac{n}{2}}, \qquad \ldots(20)$$

where n is the Steinmetz exponent. For the FX3730

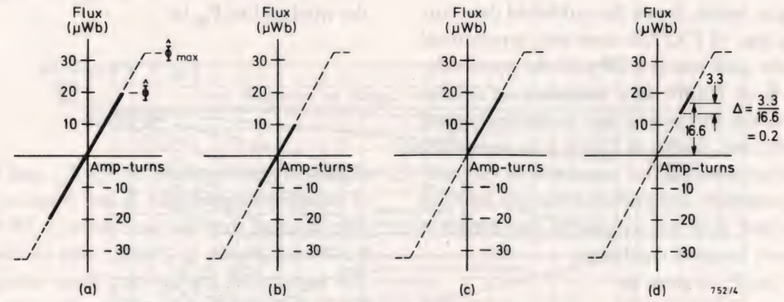


Fig.4 – Idealised magnetisation curves showing steady-state flux excursions for:
(a) balanced push-pull transformer,
(b) push-pull converter transformer with 2:1 provision for imbalance, or with lower Δ_{tr},
(c) forward converter transformer (ignoring remanence), flyback converter transformer with Δ = 1, or push-pull converter transformer as shown in (b) with some imbalance,
(d) flyback converter transformer with Δ = 0·2

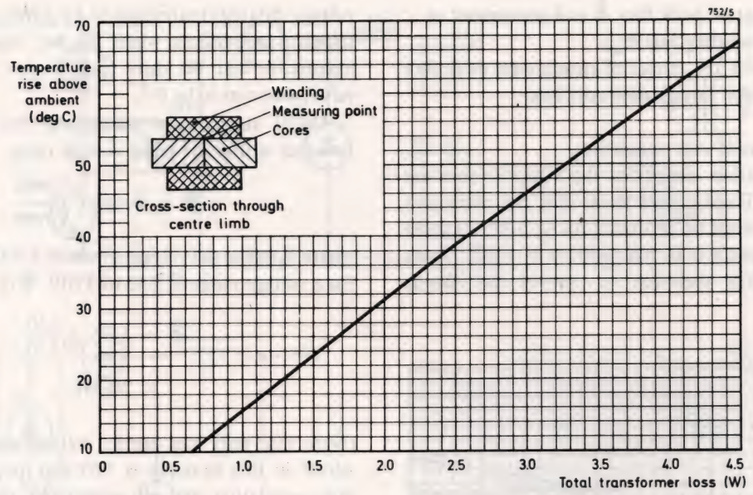


Fig.5 – Typical temperature rise of transformer using FX3730 cores as a function of total transformer loss in free-air conditions (without heatsink)

core, n = 2·5 (this is the value for type A16(3C8) ferrite material). With this value of n:

$$P_c = \frac{2{\cdot}6}{1+\frac{2{\cdot}5}{2}}, \qquad \ldots(21)$$

$$\simeq 1{\cdot}2\text{W}.$$

This is the maximum value for a transformer limited by core loss.

Peak flux $\hat{\Phi}$ and core loss, with symmetrical magnetisation

Referring to Fig.6, which shows the published data core loss curves for a pair of FX3730 cores with symmetrical magnetisation, the core loss is 1·2W with the previously-calculated flux $\hat{\Phi}$ of 20μWb at a frequency of 25kHz. Hence at 25kHz, the limitations due to saturation and core loss coincide, and 20μWb at 25kHz is an acceptable operating condition provided that imbalance in the push-pull system is prevented, and provided that the resulting magnetising current gives an acceptably low minimum d.c. output current for good regulation.

The winding loss P_w is given by:

$$P_w = P_t - P_c, \qquad \ldots(22)$$

$$= 2{\cdot}6 - 1{\cdot}2,$$

$$= 1{\cdot}4\text{W},$$

and this figure can be used in Eq.1, as will be shown in the part 'Example of use of transformer power-handling calculations'.

Reduction of $\hat{\Phi}$ to allow for imbalance in push-pull converters or to reduce Δ_{tr}

To allow for some imbalance, or to achieve a better ratio of minimum to maximum output current for good regulation (Δ_{tr}), a lower value $\hat{\Phi}$, for example 10μWb, can be selected as shown in Fig.4b. (The effect on Δ_{tr} is calculated in the next part.)

From Fig.6, the core loss P_c is 0·24W at 25kHz, and the winding loss P_w is:

$$P_w = 2{\cdot}6 - 0{\cdot}24,$$

$$= 2{\cdot}36\text{W}.$$

Graphical representation of P_c, P_w, and P_t as a function of steady-state peak flux $\hat{\Phi}$ and frequency

The values of core loss used above (1·2W for 20μWb, and 0·24W for 10μWb at 25kHz) were obtained from Fig.6. The two points representing these values are plotted in Fig.7, and solid lines are drawn from the origin through the points to represent loss against frequency. Further points read from the curves in Fig.6 at 12·5, 25, and 50kHz for given flux values are also plotted in Fig.7. These points lie on approximately straight (broken) lines in Fig.7, indicating that eddy-current losses are low, and confirming that the linear loss-against-frequency presentation gives acceptable accuracy. Fig.7 presents a useful

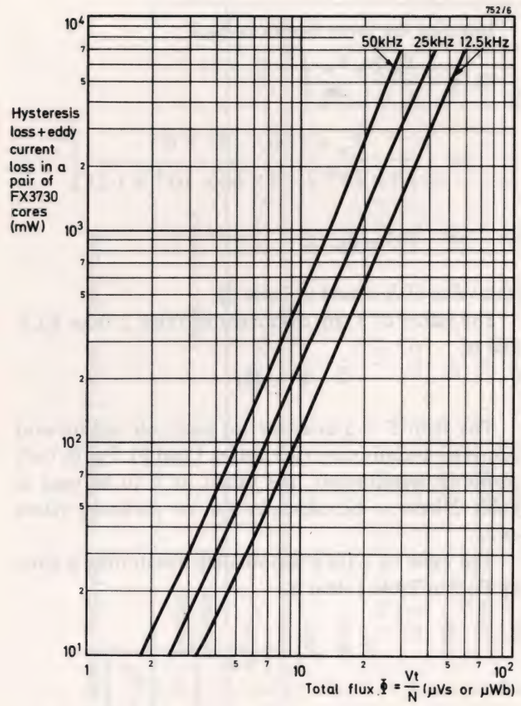


Fig.6 – Hysteresis loss and eddy-current loss as a function of total flux at 100°C, with frequency as a parameter, for a pair of FX3730 cores

picture of the magnitude of the core loss for various frequencies and operating conditions.

To calculate the winding loss, the core loss would be subtracted from the total dissipation for 40degC temperature rise given previously as 2·6W. In Fig.7, this subtraction has been performed, and when the core loss at one frequency has been obtained from the lower set of lines, the winding loss at the same frequency can be read directly from the upper set of lines.

For example, if $\hat{\Phi}$ is 20μWb, and f is 21kHz, from Fig.7 the core loss will be 1W. The winding loss is (2·6 – 1) or 1·6W. This value can be read from where the upper 20μWb line intersects with 21kHz.

The limiting value for core loss, beyond which the transformer efficiency would decrease, is indicated by the horizontal line at the previously-calculated value of 1·2W. Hence, the core loss for all possible operating conditions lies in the range from zero to 1·2W, and the permissible range of winding loss extends from 1·4W towards 2·6W.

With the aid of Fig.7, an appropriate value for $\hat{\Phi}$ can be selected for either a core-loss-limited transformer or a saturation-limited transformer, and the corresponding value of P_w is readily apparent. This value of P_w can be used in Eq.1 for both classes of transformer.

Assessment of P_c for asymmetrical magnetisation

The published data core loss curves, as shown in Fig.6, are produced for symmetrical magnetisation and are applicable for squarewave as well as sinewave voltage excitation. A problem arises, however, when the magnet-

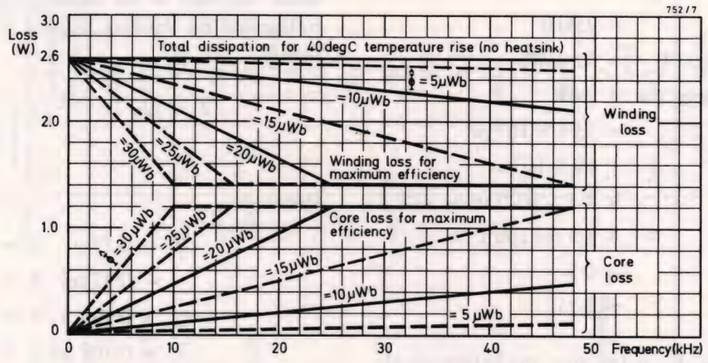


Fig.7 – Core loss P_c, winding loss P_w, and total loss P_t as a function of steady-state peak flux $\hat{\Phi}$ and frequency

isation is not symmetrical, for example in push-pull converter transformers with some degree of imbalance, or in forward or flyback converter transformers where the magnetisation is unidirectional. For these conditions, information on core loss is often not available. Without precise information, the problem can be solved in many practical instances by ignoring the imbalance and using the core loss figure that would apply if the total flux excursion were centred about zero. This figure may be 50% low. However, in the push-pull example shown in Fig.4b, with $\hat{\Phi}$ equal to 10μWb, the core loss is 0·24W which is only about 10% of the permissible winding loss of 2·36W.

Therefore, an error of 2:1 in core loss would make only 10% difference to the permissible winding loss P_w, and because P_w is among the terms influenced by the square root sign in the equation for P_o, the error in P_o would be only 5%. It follows that the same core loss figure of 0·24W can be used for the forward converter transformer (see Fig.4c) where the peak-to-peak flux excursion is the same as that in Fig.4b. Similarly, for the flyback converter transformer (see Fig.4d), if the core loss is assumed to be equal to that for symmetrical magnetisation with $\hat{\Phi}$ equal to 3·3μWb, the core loss equals 0·02W which is less than 1% of the total allowable dissipation, and this can obviously be ignored.

These approximate core loss figures for asymmetrical magnetisation are used in the next part, where an example is given of the use of the power-handling calculations.

Example of use of transformer power-handling calculations

As an example of the use of Eqs.1 to 18, P_o, $Pmin_{tr}$, and the required turns-per-volt are calculated in Table 2 for a pair of FX3730 cores. The figures shown in Table 2 are based on the FX3730 published data and the assumptions and preliminary calculations given below.

f	= 25kHz
$\hat{\Phi}$max at 100°C	= 32·2μWb
P_t for 40degC rise	= 2·6W
A_w	= 93·6 X 10^{-6} m^2
l_w	= 60 X 10^{-3} m
ρ_c	= 1·7 X 10^{-8} Ωm at 20°C
m	= 1·3 for 100°C
F_w	= 0·5
F_R	= 1·25

Note: This value of A_w is less than the total available winding area to allow for 4mm gaps between the ends of the windings and the former, giving 8mm creepage distance between the windings.

Inserting the above figures in Eq.2:

$$X = \left[\frac{P_w A_w F_w}{\rho_c m l_w F_R}\right]^{\frac{1}{2}},$$

$$= \left[\frac{P_w \times 93{\cdot}6 \times 10^{-6} \times 0{\cdot}5}{1{\cdot}7 \times 10^{-8} \times 1{\cdot}3 \times 60 \times 10^{-3} \times 1{\cdot}25}\right]^{\frac{1}{2}},$$

$$= 169\sqrt{P_w};$$

(this value of X is used in Table 2).

The values of Y are calculated in Table 2 from Eq.3, that is;

$$Y = \hat{\Phi} f.$$

The term Z is a constant for push-pull and forward converter transformers (see Tables 1 and 2). For flyback converter transformers, the values of Z to be used in Table 2 have to be calculated for the particular values of Δ.

The value of Z for a two-winding transformer is given by Eq.9 in Table 1; that is:

$$Z = \sqrt{2} \cdot \frac{\Delta}{1+\Delta} \cdot \frac{1}{\left[1+\frac{\Delta^2}{3}\right]^{\frac{1}{2}}}.$$

Therefore:

$$Z = 0{\cdot}61 \text{ for } \Delta = 1,$$
$$= 0{\cdot}45 \text{ for } \Delta = 0{\cdot}5,$$
$$= 0{\cdot}23 \text{ for } \Delta = 0{\cdot}2,$$
$$= 0{\cdot}13 \text{ for } \Delta = 0{\cdot}1.$$

Note: The values of 1, 0·5, 0·2, and 0·1 for Δ are arbitrarily chosen to demonstrate the effect of Δ on P_o.

The value of Z for a three-winding transformer in which one-third of the winding space is occupied by a voltage-limiting winding is given by Eq.11 in Table 1, that is:

$$Z = 2/\sqrt{3} \cdot \frac{\Delta}{1+\Delta} \cdot \frac{1}{\left[1+\frac{\Delta^2}{3}\right]^{\frac{1}{2}}}.$$

Therefore:

$$Z = 0{\cdot}5 \text{ for } \Delta = 1,$$
$$= 0{\cdot}37 \text{ for } \Delta = 0{\cdot}5,$$
$$= 0{\cdot}19 \text{ for } \Delta = 0{\cdot}2,$$
$$= 0{\cdot}105 \text{ for } \Delta = 0{\cdot}1.$$

To calculate $Pmin_{tr}$ for a push-pull converter transformer, where $Pmin_{tr}$ is $\Delta_{tr}P_o$, the value of Δ_{tr} is required.

TABLE 2

Example of Calculations for Transformers using FX3730 Cores in Push-pull, Forward, and Flyback Converters

Term, or calculation	Unit	Push-pull converter			Forward converter		Flyback converter											
		Balanced $\hat{\Phi}$ = 20μWb		SF = 2 $\hat{\Phi}$ = 10μWb			Δ = 1		Δ = 0·5		Δ = 0·2		Δ = 0·1					
$V_i$max		370		370	370		370		370		370		370					
$V_i$min (for δ = 0·5)		230		230	230		230		230		230		230					
$a = V_i max/V_i min$		1·61		1·61	1·61		1·61		1·61		1·61		1·61					
$\hat{\Phi}$max	μWb	32·2		32·2	32·2		32·2		32·2		32·2		32·2					
$\hat{\Phi} = \hat{\Phi}$ max/a SF	μWb	20		10	20		20		20		20		20					
P_c	W	1·2		0·24	0·24		0·24		0		0		0					
T_{max}	°C	100		100	100		100		100		100		100					
T_{amb}	°C	60		60	60		60		60		60		60					
T_{rise}	degC	40		40	40		40		40		40		40					
P_t	W	2·6		2·6	2·6		2·6		2·6		2·6		2·6					
$P_w = P_t - P_c$	W	1·4		2·36	2·36		2·36		2·6		2·6		2·6					
$X = 169\sqrt{P_w}$		200		260	260		260		272		272		272					
$Y = \hat{\Phi}f$		0·5		0·25	0·5		0·5		0·5		0·5		0·5					
XY		100		65	130		130		136		136		136					
Number of windings																		
Z		2 3 4		2 3 4	2 3		2 3		2 3		2 3		2 3					
P_o = XYZ	W	200 163 141		130 106 92	92 75		79 65		61 50		32 26		17·5 14·3					
Δ_{tr}		0·117	0·144	0·166	0	0	1	1	0·5	0·5	0·2	0·2	0·1	0·1	0·065	0·063	0·055	0·045
$Pmin_{tr} = \Delta_{tr} P_o$	W	23·4	23·4	23·4	0	0	79	65	30·5	25	6·4	5·2	1·75	1·43	5·8	5·8	5·8	5·8
$Pmin_{tr}$ (typical value assuming μ_a typ = 2μ_a min)	W	11·7	11·7	11·7											2·9	2·9	2·9	2·9
Turns per volt at $V_i$min		0·5	0·5	0·5	1·0	1·0	1·0	1·0	1·5	1·5	3	3	5·5	5·5	1·0	1·0	1·0	1·0

From the FX3730 published data, the core factor C_1 is given as $0{\cdot}735mm^{-1}$. Therefore:

$$\frac{\ell_e}{A_e} = C_1, \qquad \ldots(23)$$

$$= 0{\cdot}735mm^{-1},$$

$$= 735m^{-1}.$$

The relative amplitude permeability μ_a for FX3730 cores is 1000min. Hence, for the push-pull transformer with flux $\hat{\Phi}$ equal to 20μWb:

$$\Delta_{tr} = \frac{\hat{\Phi}}{XZ} \cdot \frac{\ell_e}{A_e} \cdot \frac{1}{\mu_a} \cdot \frac{10^7}{\pi}; \qquad \ldots(24)$$

using value of X from Table 2:

$$\Delta_{tr} = \frac{20 \times 10^{-6}}{200Z} \times 735 \times \frac{1}{1000} \times \frac{10^7}{\pi},$$

$$= \frac{0{\cdot}234}{Z}.$$

Δ_{tr} = 0·117 for the two-winding push-pull converter transformer,

= 0·144 for the three-winding push-pull converter transformer,

= 0·166 for the four-winding push-pull converter transformer.

For a push-pull transformer with flux $\hat{\Phi}$ equal to 10μWb:

$$\Delta_{tr} = \frac{10 \times 10^{-6}}{260Z} \times 735 \times \frac{1}{1000} \times \frac{10^7}{\pi},$$

$$= \frac{0{\cdot}09}{Z}.$$

Δ_{tr} = 0·045 for the two-winding push-pull converter transformer,

= 0·055 for the three-winding push-pull converter transformer,

= 0·063 for the four-winding push-pull converter transformer.

The Δ_{tr} values given above for push-pull converter transformers are used in Table 2. For forward converter transformers, Δ_{tr} = 0. The Δ_{tr} values given in Table 2 for flyback converter transformers are equal to the arbitrary values chosen as design requirements.

Notes on accuracy of calculations

With the aid of Eqs.1 to 13, the power-handling capability of all types of output transformer and choke used in squarewave d.c.-to-d.c. converters can be calculated. Because flux density is chosen, and core loss is assessed before output power is calculated, separate equations for transformers limited by saturation and transformers limited by core loss are avoided, and the calculations are simple.

Approximations in derivations of equations

To retain simplicity, three approximations are used in the derivations of Eq.1. The first approximation is that input and output powers are equal. This first approximation is justified, because most transformers and chokes used in SMPS converters have typical efficiencies of about 97%.

The second approximation is that power loss due to magnetising current in the windings of push-pull and forward converter transformers is assumed to be negligible in comparison with the power loss due to load current. The error in winding loss in a push-pull transformer with 10% magnetising current is about 0·3%, which is negligible. In a forward converter in which the peak magnetising current is 10% of the load current, the error in winding loss would be about 10%, which corresponds to errors of up to 10% for temperature rise, or 5% for output power.

The third approximation, applicable to flyback converter transformers and chokes, is that magnetising current and flux are linearly related. Because flyback transformers and chokes have large core gaps, the assumption of linearity is justified. For chokes which are normally designed to operate up to the maximum possible flux density, the most accurate inductance figure for a given current can be obtained from Hanna curves, which are in any case needed to determine the gap. Output power figures calculated from Hanna curve information will, however, be very similar to those calculated from maximum flux density information, as in this article. An important feature of chokes is that they must not saturate at the maximum current available from the short-circuited power supply, and this depends on the protection system employed. The power-handling capability of an output choke must therefore always be greater than the rated power output of the supply.

Accuracy of core data and winding data

As shown above, errors due to approximations used in the derivations of Eq.1 are generally small, and for a specific design any errors can be easily corrected if so desired. The accuracy of results therefore depends on the accuracy of the data employed. The circuit designer can

specify the relevant application requirements, taking into account circuit losses and practical limitations on duty cycle, etc Four significant items remain which could be sources of error. These items are the total dissipation in the component for a given temperature rise, the core loss, the a.c.-to-d.c. resistance ratio of the windings, and the ratio of copper-to-window area.

The figure for dissipation against temperature rise is best obtained experimentally, or from experimentally-based data, because this data can give the effective thermal resistance from the hottest point (between the windings and the core) and the ambient, taking into account the complex thermal paths through the core and the windings.

Accurate core loss information for symmetrical magnetisation is generally available. For asymmetrical magnetisation, core losses often contribute only a small part of the total loss, and so an adequate assessment of core losses can be made for many applications by using the data based on symmetrical magnetisation. At higher frequencies, however, such as 50kHz, where core losses with asymmetrical magnetisation become significant, more accurate information may be necessary. Similarly, for greatest accuracy in the calculation of forward converter transformers (which do not usually have gapped cores), the remanent flux should be taken into account in determining the permissible flux excursion. However, in forward converters in which the rate of rise of transistor collector voltage is limited by a 'slow-rise' capacitor, the discharge current of this capacitor will tend to reduce the remanent flux to zero.

In the initial selection of a core for a given application, the a.c.-to-d.c. resistance ratio F_R in the windings, and the ratio F_w of copper area to window area, are not known. Therefore, figures for F_R and F_w based on experience must be used. It is suggested that a figure of 0·4 for F_w/F_R is typical for most well-designed windings on cores having window dimensions designed specifically for high-frequency applications. (On other cores which may allow excessive winding height it may be necessary to underfill the winding area to achieve an acceptable value of F_R, and this would have to be taken into account by using a low value of F_w, and possibly also reducing the figure for total allowable dissipation.) Subject to these conditions for the core and windings, the figure of 0·4 for F_w/F_R is likely to be accurate to within ±20%, and because the expression F_w/F_R is influenced by a square root sign in Eq.2, an equation which determines the value of P_o, the initial figure for output power is likely to be accurate to within ±10%. Assuming that the initial figure is acceptable, detailed design can then proceed using the high-frequency winding design procedure described in Refs.3, 4, and 5, and the figure for P_o can be very simply corrected when the final values for F_w and F_R are known.

Variation of P_o with operating conditions

It will be noted that all calculations have been carried out at a minimum d.c. supply voltage where the duty cycle is equal to 0·5. In some converter designs, the maximum value of δ may be limited to, for example, 0·45, which would correspond to a practical minimum supply voltage slightly higher than the value of $V_i$min used here. In addition, temperature rise measurements may sometimes be carried out at the nominal supply voltage, which may be well above the minimum value. From Appendices 2 and 3 for push-pull and forward converter transformers, the output power obtainable for a given temperature rise at supply voltages above the minimum value $V_i$min where δ is equal to 0·5 is given by:

$$P_o' = P_o \sqrt{(0{\cdot}5/\delta)}, \qquad \ldots(25)$$

where P_o' is the transformer output power for a given value of δ, and P_o is the transformer output power for δ = 0·5 as given by Eq.1.

Alternatively, since $\delta = 0{\cdot}5\,(V_i\text{min}/V_i)$, power output P_o' can be expressed as:

$$P_o' = P_o \sqrt{(V_i/V_i\text{min})}. \qquad \ldots(26)$$

From Appendix 4, it will be seen that the value of P_o for a flyback converter transformer is independent of the value of δ for which the converter is designed. For a given converter design, however, in which the transformer inductance has been fixed, P_o and $P_o$min vary as the supply voltage and duty cycle are varied. These variations are not calculated in this article, and so the figures for P_o and $P_o$min apply strictly to the minimum supply voltage condition where δ was fixed. In Appendix 5, which deals with chokes, supply voltage and δ are taken into account in the derivation of P_o. Operational variations are therefore fully covered by the term Z in the power-handling equations for chokes.

Laboratory results

Experiments to date with push-pull converter transformers, forward converter transformers, and chokes, have shown that when all relevant factors are taken into account, the measured figures for transformer temperature rise in practical circuits agree with the theoretical predictions to within about ±10%.

ACKNOWLEDGEMENTS

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article is based. The author is also indebted to E.C. Snelling of Mullard Research Laboratories, whose book 'Soft Ferrites, Properties and Applications' was used as a constant reference throughout the work.

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4. SNELLING, E.C., 'Soft Ferrites, Properties and Applications', Iliffe Books Ltd., London, 1969.
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The terms used in the calculations in the appendices are defined in the section 'Symbols and definitions'.

APPENDIX 1

Calculation of Permissible Total Ampere-turns for a Given Power Loss in the Windings

The total effective cross-sectional area of the copper in the windings is given by:

$$A_w F_w U_F. \quad \ldots (27)$$

Fig.8 shows the relationship of A_w, F_w, and U_F to the construction of the windings.

The total effective resistance in the utilised windings R_u is given by:

$$R_u = \rho_c m F_R \left(\frac{\frac{N_u l_w}{A_w F_w U_F}}{N_u} \right),$$

$$= \frac{\rho_c m F_R N_u^2 l_w}{A_w F_w U_F}. \quad \ldots (28)$$

The total power loss P_w in the windings is given by:

$$P_w = I^2_{rms} R_u.$$

Therefore:

$$P_w = I^2_{rms} \left(\frac{\rho_c m F_R N_u^2 l_w}{A_w F_w U_F} \right) \quad \ldots (29)$$

In practice, P_w is determined by the permissible temperature rise and the core loss, and so the maximum permissible total number of ampere-turns is given by:

$$I_{rms} N_u = \left[\frac{P_w A_w F_w U_F}{\rho_c m l_w F_R} \right]^{\frac{1}{2}}. \quad \ldots (30)$$

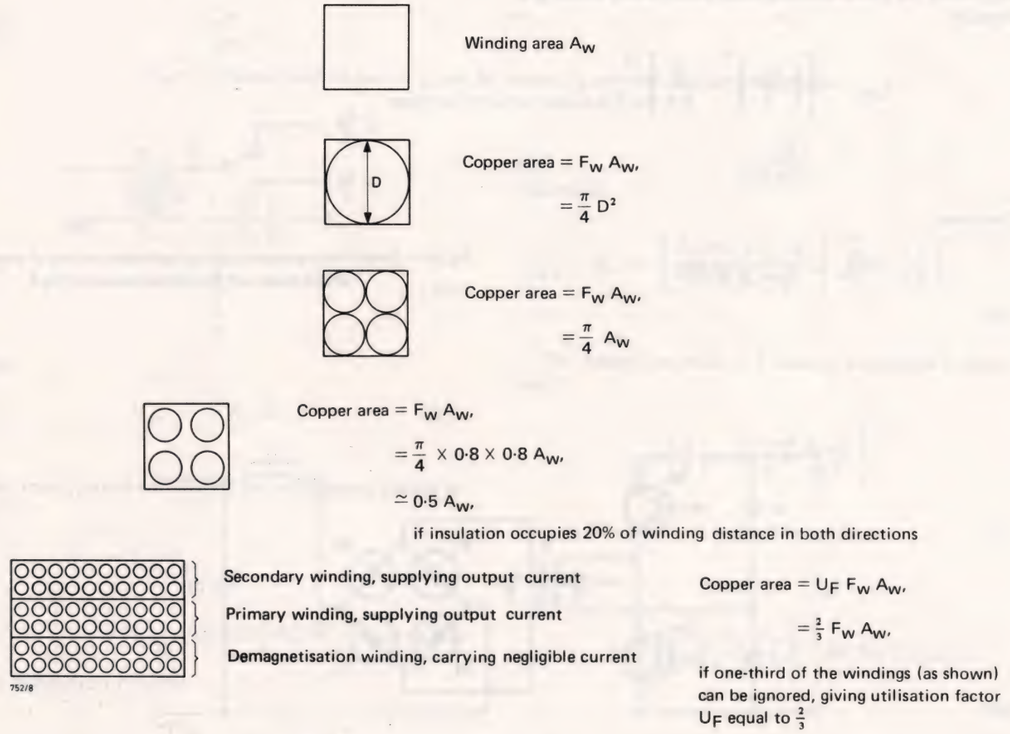

Winding area A_w
D
Copper area = $F_w A_w$,
$= \frac{\pi}{4} D^2$
Copper area = $F_w A_w$,
$= \frac{\pi}{4} A_w$
Copper area = $F_w A_w$,
$= \frac{\pi}{4} \times 0{\cdot}8 \times 0{\cdot}8 A_w$,
$\simeq 0{\cdot}5 A_w$,
if insulation occupies 20% of winding distance in both directions
Secondary winding, supplying output current
Primary winding, supplying output current
Demagnetisation winding, carrying negligible current
752/8
Copper area = $U_F F_w A_w$,
$= \frac{2}{3} F_w A_w$,
if one-third of the windings (as shown) can be ignored, giving utilisation factor U_F equal to $\frac{2}{3}$

Fig.8 – Relationship of terms A_w, F_w, and U_F to construction of windings

APPENDIX 2

Two-winding, Three-winding, and Four-winding Push-pull Converter Transformers

TWO-WINDING PUSH-PULL CONVERTER TRANSFORMER

A single-ended push-pull converter with a bridge-rectified output is shown in Fig.9. A simplified representation of the switching action of this converter is shown in Fig.10. Waveforms of current I_p (Fig.11a), and voltage V_p and total flux (Fig.11b), are shown for the converter of Fig.9. The following calculations are also applicable to the two-winding transformer in the converter with full bridge drive and bridge-rectified output, as shown in Fig.1b.

The primary current I_p (ignoring magnetising current) of the transformer shown in Fig.9 is a squarewave of amplitude I_{dc}/δ, where δ is the transistor duty cycle having a maximum value of 0·5. For a 1:1 turns ratio, the secondary current is identical to the primary current and, as mentioned in the Introduction, practical turns ratios do not affect the power-handling capability of transformers, provided that the required packing factors and a.c.-to-d.c. resistance ratios are achieved in practice. Therefore, the r.m.s. current in all parts of the winding is given by:

$$I_{rms} = \left[\left(\frac{I_{dc}}{\delta}\right)^2 \cdot \frac{\delta}{0{\cdot}5}\right]^{\frac{1}{2}},$$

$$= \frac{I_{dc}}{\sqrt{(0{\cdot}5\delta)}}. \qquad \ldots(31)$$

Therefore:

$$I_{dc} = I_{rms}\sqrt{(0{\cdot}5\delta)}. \qquad \ldots(32)$$

The maximum permissible volts-per-turn is determined by:

$$V = N\frac{d\Phi}{dt},$$

or

$$\frac{V}{N} = \frac{d\Phi}{dt}. \qquad \ldots(33)$$

For the converter shown in Fig.9:

$$V_p = \frac{V_{dc}}{2},$$

and

$$N_p = \frac{N_u}{2}.$$

Therefore:

$$\frac{V_p}{N_p} = \frac{V_{dc}}{2} \cdot \frac{2}{N_u},$$

$$= \frac{V_{dc}}{N_u}, \qquad \ldots(34)$$

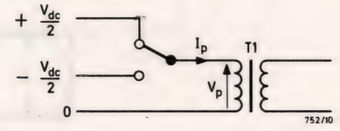


Fig.10 — Simplified representation of switching action of single-ended push-pull converter shown in Fig.9

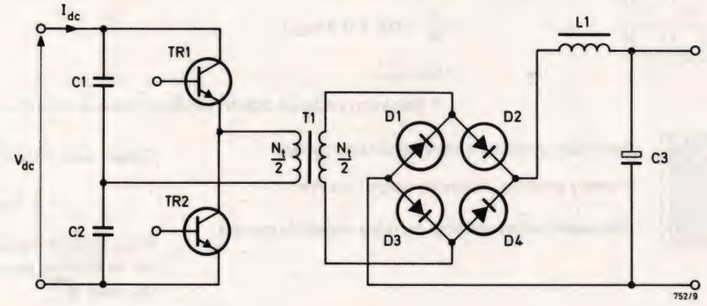


Fig.9 — Single-ended push-pull converter with bridge-rectified output

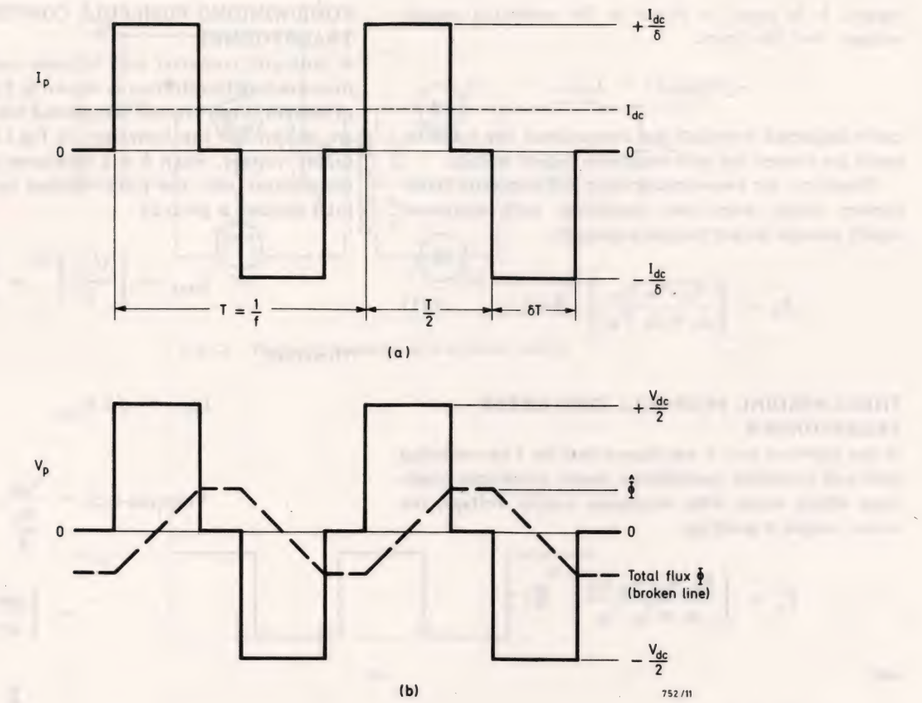


Fig.11 — Waveforms of (a) current I_p, and (b) voltage V_p and total flux, for single-ended push-pull converter shown in Fig.9

and

$$\frac{V_{dc}}{N_u} = \left[\frac{d\Phi}{dt}\right],$$

$$= \frac{\hat{\Phi}}{\frac{\delta}{2f}}, \qquad \ldots(35)$$

that is:

$$V_{dc} = \frac{2}{\delta} N_u \hat{\Phi} f. \qquad \ldots(36)$$

The input power (or output power ignoring losses) is given by:

$$P_o = I_{dc}\, V_{dc},$$

$$= I_{rms}\sqrt{(0{\cdot}5\delta)}\,\frac{2}{\delta} N_u \hat{\Phi} f. \qquad \ldots(37)$$

From Appendix 1 (Eq.30):

$$I_{rms}\, N_u = \left[\frac{P_w\, A_w\, F_w\, U_F}{\rho_c\, m\, l_w\, F_R}\right]^{\frac{1}{2}}.$$

Therefore:

$$P_o = \left[\frac{P_w\, A_w\, F_w\, U_F}{\rho_c\, m\, l_w\, F_R}\right]^{\frac{1}{2}} \hat{\Phi} f \sqrt{\left(\frac{2}{\delta}\right)}. \qquad \ldots(38)$$

The maximum value of δ (that is, δmax) is 0·5. Therefore:

$$\sqrt{\left(\frac{2}{\delta}\right)} = \left[\frac{2}{\delta} \times \frac{\delta\text{max}}{0{\cdot}5}\right]^{\frac{1}{2}},$$

$$= 2\sqrt{(\delta\text{max}/\delta)}. \qquad \ldots(39)$$

Therefore:

$$P_o = \left[\frac{P_w\, A_w\, F_w\, U_F}{\rho_c\, m\, l_w\, F_R}\right]^{\frac{1}{2}} \hat{\Phi} f\, 2\sqrt{(\delta\text{max}/\delta)}. \qquad \ldots(40)$$

Since the total winding is fully utilised, U_F is equal to 1. Additionally, in a conventional constant-voltage power

supply, δ is equal to δmax at the minimum supply voltage, and the term:

$$\sqrt{(\delta \max/\delta)} = 1$$

can be neglected, provided that temperature rise measurements are carried out with minimum supply voltage.

Therefore, for two-winding push-pull converter transformers under worst-case conditions, with minimum supply voltage, power output is given by:

$$P_o = \left[\frac{P_w A_w F_w}{\rho_c m l_w F_R}\right]^{\frac{1}{2}} \hat{\Phi} f 2. \quad \ldots (41)$$

THREE-WINDING PUSH-PULL CONVERTER TRANSFORMER

In the previous part it was shown that for a two-winding push-pull converter transformer, under worst-case conditions which occur with minimum supply voltage, the power output is given by:

$$P_o = \left[\frac{P_w A_w F_w U_F}{\rho_c m l_w F_R}\right]^{\frac{1}{2}} \hat{\Phi} f 2,$$

and

$$U_F = 1.$$

Three-winding transformers with a bi-phase secondary (see Figs.1c and 1d), or a bi-phase primary (see Fig.1e), can be regarded as being identical to the two-winding push-pull converter transformer. These three-winding transformers have only two active windings, one primary and one secondary, because during every half-cycle one of the three windings is inactive. Assuming that each of the windings occupies one-third of the winding space*, U_F is equal to $\frac{2}{3}$. Hence the output power for a three-winding push-pull converter transformer is given by:

$$P_o = \left[\frac{P_w A_w F_w}{\rho_c m l_w F_R}\right]^{\frac{1}{2}} \hat{\Phi} f 2\sqrt{(2/3)}. \quad \ldots (42)$$

*For a three-winding transformer having the same F_R and F_w values for the primary and the secondary, the single winding should occupy $\sqrt{(2)}-1$ or 41·4% of the winding space for maximum efficiency, and the remaining two windings should each occupy 29·3% of the space. Eq.42 yields a value for P_o which is accurate, nowever, for transformers where the single winding occupies either one-third or one-half of the winding space, and the error in P_o does not exceed 1·5% for values between one-third and one-half.

FOUR-WINDING PUSH-PULL CONVERTER TRANSFORMER

A push-pull converter with bi-phase output and using a four-winding transformer is shown in Fig.12. Waveforms of current (Fig.13a), and voltage and total flux (Fig.13b), are shown for the converter of Fig.12. For minimum supply voltage, when δ is a maximum giving maximum temperature rise, the r.m.s. current in all parts of the total winding is given by:

$$I_{rms} = \left[\frac{I^2_{dc}}{2}\right]^{\frac{1}{2}} = \frac{I_{dc}}{\sqrt{2}}. \quad \ldots (43)$$

Therefore:

$$I_{dc} = \sqrt{2}\, I_{rms}.$$

$$\text{Volts-per-turn} = \frac{V_{dc}}{\frac{N_t}{4}},$$

$$= \left[\frac{d\Phi}{dt}\right],$$

$$= \frac{\hat{\Phi}}{\frac{1}{4f}},$$

$$= \hat{\Phi} 4f.$$

Therefore:

$$V_{dc} = \hat{\Phi} f N_t, \quad \ldots (44)$$

and

$$P_o = I_{dc} V_{dc},$$

$$= \sqrt{2}\, I_{rms} \hat{\Phi} f N_t. \quad \ldots (45)$$

From Appendix 1, using the value of $I_{rms} N_u$ given in Eq.30, and with U_F equal to 1:

$$P_o = \left[\frac{P_w A_w F_w}{\rho_c m l_w F_R}\right]^{\frac{1}{2}} \hat{\Phi} f \sqrt{2}. \quad \ldots (46)$$

Note that the same result can be obtained by regarding the four-winding transformer in Fig.12 as having two windings which are active during every half-cycle, and two windings which are inactive. When the four-winding transformer is considered in this way, $N_u = N_t/2$, and $U_F = \frac{1}{2}$. The result from Eq.46 can be obtained by multiplying the result from Eq.41 for a two-winding push-pull transformer by $\sqrt{(1/2)}$.

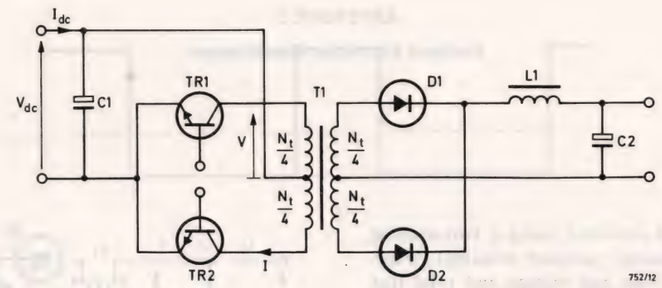


Fig.12 – Push-pull converter with bi-phase output

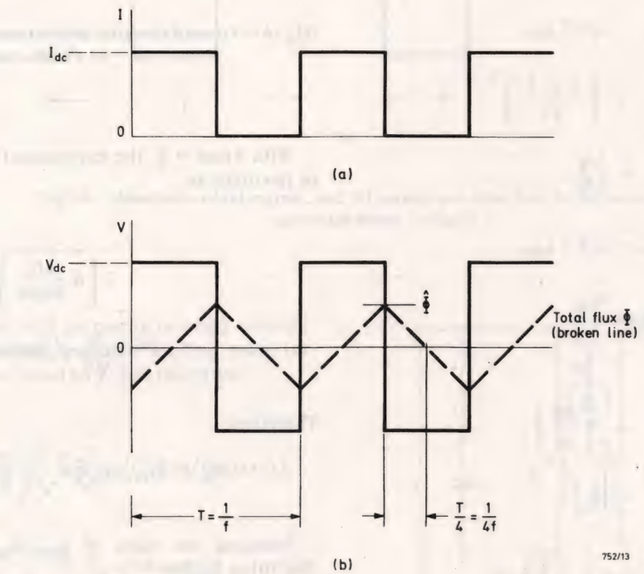


Fig.13 – Waveforms of (a) current, and (b) voltage and total flux, for push-pull converter with bi-phase output shown in Fig.12

APPENDIX 3

Forward Converter Transformers

Fig.14 shows a forward converter using a two-winding transformer (without energy recovery winding). Waveforms of current (Fig.15a), and voltage and total flux (Fig.15b), are shown for the converter of Fig.14. Ignoring the magnetising current, the input current to the converter is given by:

$$I \delta T = I_{dc} T. \qquad \ldots (47)$$

Therefore:

$$I = \frac{I_{dc}}{\delta}.$$

Additionally:

$$I_{rms} = \sqrt{(I^2 \delta)},$$

$$= \left[\frac{I^2_{dc} \delta}{\delta^2} \right]^{1/2}.$$

Therefore:

$$I_{rms} = \frac{I_{dc}}{\sqrt{\delta}},$$

from which:

$$I_{dc} = \sqrt{\delta} \cdot I_{rms}.$$

$$\text{Volts-per-turn} = \frac{V_{dc}}{\frac{N_u}{2}},$$

$$= \left[\frac{d\Phi}{dt} \right],$$

$$= \hat{\Phi} \frac{f}{\delta}.$$

Therefore:

$$V_{dc} = \hat{\Phi} \frac{f}{\delta} \cdot \frac{N_u}{2}. \qquad \ldots (48)$$

Note that for the forward converter transformer:

$$\hat{\Phi} = (\text{maximum flux}) - (\text{remanent flux}).$$

The power-handling capability P_o is given by:

$$P_o = I_{dc} V_{dc},$$

$$= \sqrt{\delta}\, I_{rms} \hat{\Phi} \frac{f}{\delta} \frac{N_u}{2},$$

$$= I_{rms} N_u \hat{\Phi} f \frac{1}{2\sqrt{\delta}}. \qquad \ldots (49)$$

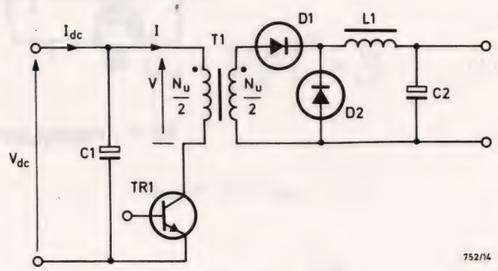


Fig.14 — Forward converter without energy recovery winding on transformer T_1

With $\delta max = \frac{1}{2}$, the expression $(1/2\sqrt{\delta})$ in Eq.49 can be rewritten as:

$$\frac{1}{2\left[\delta \frac{1/2}{\delta max}\right]^{1/2}},$$

$$= \frac{1}{\sqrt{2}} \sqrt{(\delta max/\delta)}.$$

Therefore:

$$P_o = I_{rms} N_u \hat{\Phi} f \frac{1}{\sqrt{2}} \sqrt{(\delta max/\delta)}. \qquad \ldots (50)$$

Inserting the value of $I_{rms} N_u$ from Appendix 1 (Eq.30) in Eq.50:

$$P_o = \left[\frac{P_w A_w F_w U_F}{\rho_c m l_w F_R} \right]^{1/2} \hat{\Phi} f \frac{1}{\sqrt{2}} \sqrt{(\delta max/\delta)}. \qquad \ldots (51)$$

For a forward converter transformer without an energy recovery winding (as shown in Fig.14), where the total winding space is fully utilised to supply output current, the utilisation factor U_F is equal to 1, and therefore:

$$P_o = \left[\frac{P_w A_w F_w}{\rho_c m l_w F_R} \right]^{1/2} \hat{\Phi} f \frac{1}{\sqrt{2}} \sqrt{(\delta max/\delta)}. \qquad \ldots (52)$$

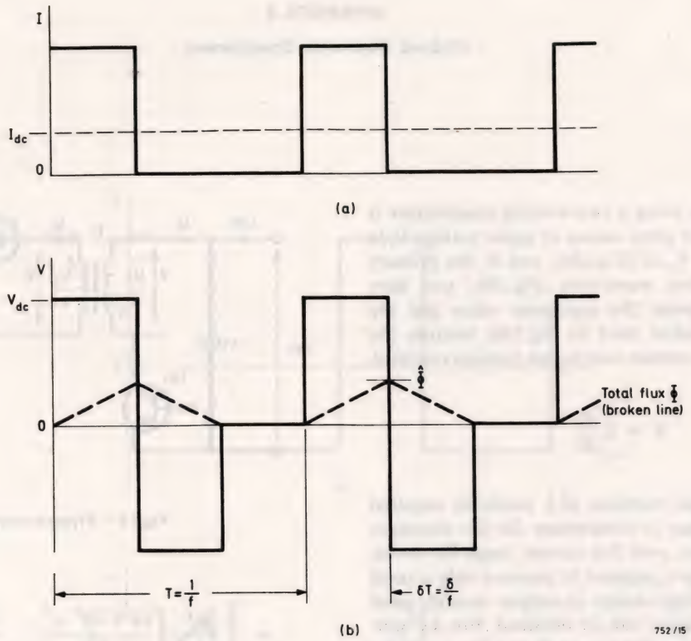


Fig.15 — Waveforms of (a) current, and (b) voltage and total flux, for forward converter shown in Fig.14

For the transformer with an energy recovery winding occupying one-third of the available winding space (as shown in Fig.16), U_F is equal to $\frac{2}{3}$, and therefore:

$$P_o = \left[\frac{P_w A_w F_w}{\rho_c m l_w F_R} \right]^{1/2} \hat{\Phi} \frac{1}{\sqrt{2}} \sqrt{(2/3)} \sqrt{(\delta max/\delta)},$$

$$= \left[\frac{P_w A_w F_w}{\rho_c m l_w F_R} \right]^{1/2} \hat{\Phi} \frac{1}{\sqrt{3}} \sqrt{(\delta max/\delta)}. \qquad \ldots (53)$$

For the forward converters with or without an energy recovery winding, P_o is minimum, or temperature rise is maximum, when the supply voltage is minimum and $\delta = \delta max$. The term $\sqrt{(\delta max/\delta)}$ can be omitted for the evaluation of worst-case conditions.

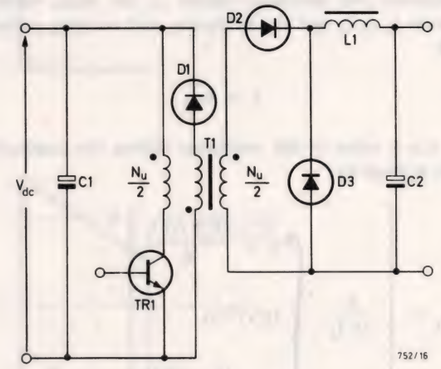


Fig.16 — Forward converter with energy recovery winding on transformer T_1. The utilisation factor $U_F = \frac{2}{3}$ if the three windings occupy equal areas

APPENDIX 4

Flyback Converter Transformer

A flyback converter using a two-winding transformer is shown in Fig.17. For given values of input voltage $V_i dc$ and output voltage $V_o dc$ (Fig.18a), and δ, the primary and secondary current waveforms (Fig.18b) may have any amplitude between the maximum value and the minimum value (broken line) in Fig.18b, because the slope on top of the current waveforms remains constant, and the expression:

$$V = L\frac{di}{dt}$$

is satisfied.

In practice, a small variation of δ would be required over this current range to compensate for the change in circuit losses. Because over this current range the power supply feedback loop is required to produce only a small change in δ for a large change in output current, good output voltage regulation can be obtained. For d.c. output currents lower than the mean value of the minimum secondary current (shown by the broken line in Fig.18b), δ must be reduced to avoid a large increase in output voltage, giving poorer regulation.

The r.m.s. value of the current waveforms in Fig.18b can be derived with reference to Fig.19. Defining the maximum and minimum values of the mean value of current I_s as I_s and ΔI_s as shown, and erecting scales so that:

$$I = Kx,$$

the r.m.s. value of the waveform during the conduction time is given by:

$$I_{rms} = \left[\frac{K}{2\Delta I_s}\int_{x=\frac{(1-\Delta)I_s}{K}}^{x=\frac{(1+\Delta)I_s}{K}} (Kx)^2\,dx\right]^{\frac{1}{2}},$$

$$= \left[\frac{K^3}{2\Delta I_s}\left[\frac{x^3}{3}\right]_{x=\frac{(1-\Delta)I_s}{K}}^{x=\frac{(1+\Delta)I_s}{K}}\right]^{\frac{1}{2}},$$

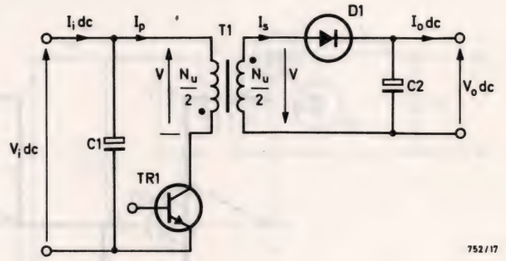


Fig.17 – Flyback converter

$$= \left[\frac{K^3}{6\Delta I_s}\left(\frac{(1+\Delta)^3 I_s^3}{K^3} - \frac{(1-\Delta)^3 I_s^3}{K^3}\right)\right]^{\frac{1}{2}},$$

$$= I_s\left[\frac{1}{6\Delta}\left\{(1+3\Delta+3\Delta^2+\Delta^3) - (1-3\Delta+3\Delta^2-\Delta^3)\right\}\right]^{\frac{1}{2}},$$

$$= I_s\left[1+\frac{\Delta^2}{3}\right]^{\frac{1}{2}}. \quad \ldots(54)$$

Assuming equal numbers of primary and secondary turns, the mean values of currents I_p and I_s during their respective conduction times are equal, and the primary and secondary resistances are each equal to $R_u/2$, where R_u is the resistance of the total number of utilised turns N_u. Then:

$$\text{primary loss} = I_p^2\left(1+\frac{\Delta^2}{3}\right)\frac{R_u}{2}\delta, \quad \ldots(55)$$

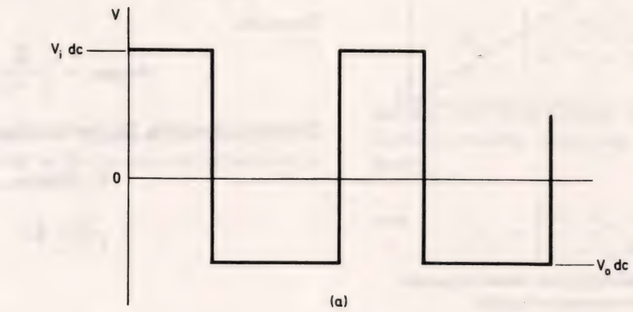
$$= I_s^2\left(1+\frac{\Delta^2}{3}\right)\frac{R_u}{2}\delta,$$

and

$$\text{secondary loss} = I_s^2\left(1+\frac{\Delta^2}{3}\right)\frac{R_u}{2}(1-\delta). \quad \ldots(56)$$

Therefore:

$$\text{total loss} = \frac{I_s^2}{2}\left(1+\frac{\Delta^2}{3}\right)R_u. \quad \ldots(57)$$



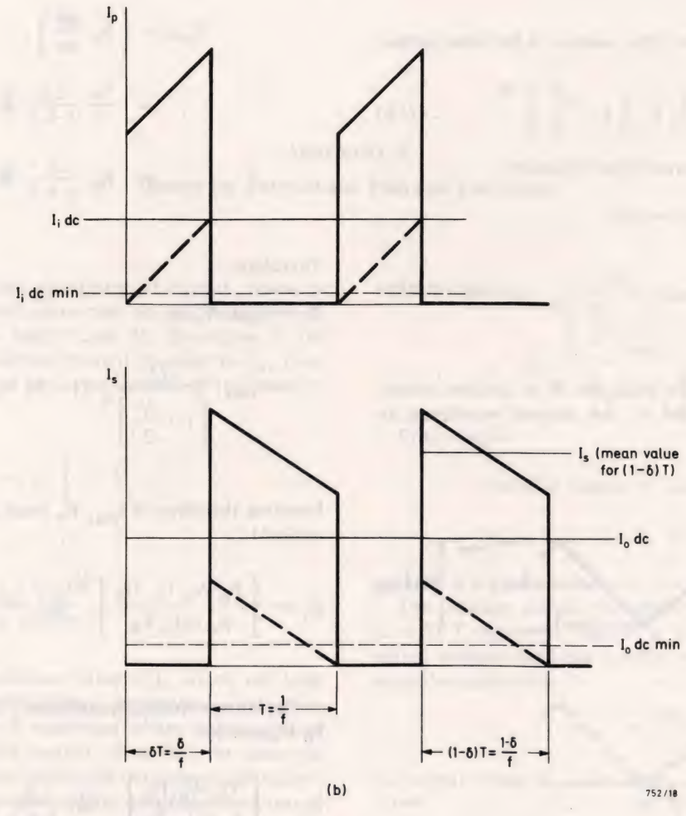


Fig.18 – Waveforms of (a) voltage and (b) current for flyback converter shown in Fig.17

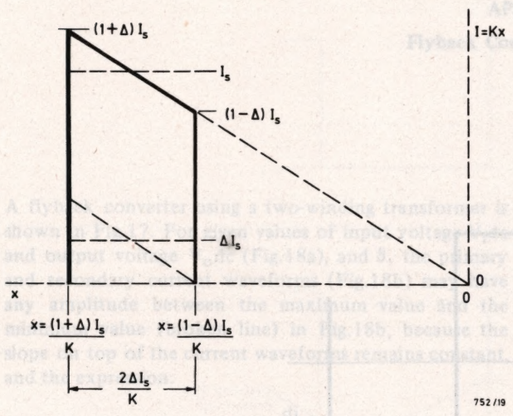


Fig.19 — Construction for deriving r.m.s. values of current waveforms shown in Fig.18b

Therefore the effective r.m.s. current in the total utilised winding is given by:

$$I_{rms} = \frac{1}{\sqrt{2}} I_s \left[1 + \frac{\Delta^2}{3}\right]^{\frac{1}{2}} . \quad \ldots (58)$$

The d.c. output current $I_o dc$ is given by:

$$I_o dc = I_s (1-\delta),$$

$$= I_{rms} \frac{\sqrt{2}}{\left[1 + \frac{\Delta^2}{3}\right]^{\frac{1}{2}}} (1-\delta). \quad \ldots (59)$$

The waveform of the total flux Φ in the core, shown in Fig.20, is the same as the current waveforms in Figs.18b and 19. (Since flyback converter transformer cores are normally gapped, the assumption of a linear relationship between flux and current is justified.)

From Fig.20, the peak flux $\hat{\Phi}$ (under steady-state operating conditions) is equal to:

$$(1 + \Delta)\, \Phi mean.$$

Therefore:

$$\Phi mean = \frac{\hat{\Phi}}{1+\Delta}.$$

Therefore, from Fig.20, the total flux change is equal to:

$$2\Delta\, \Phi mean,$$

$$= \frac{2\Delta}{1+\Delta} \hat{\Phi}.$$

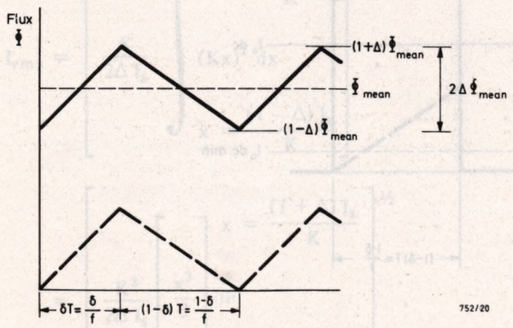


Fig.20 — Flux waveform for flyback converter transformer (or choke)

The output voltage $V_o dc$ is given by:

$$V_o dc = \left(N_s \frac{d\Phi}{dt}\right),$$

$$= \frac{N_u}{2} \frac{2\Delta}{1+\Delta} \hat{\Phi} \frac{f}{1-\delta}, \quad \ldots (60)$$

Therefore:

$$P_o = I_o dc\, V_o dc,$$

$$= I_{rms} \frac{\sqrt{2}}{\left[1 + \frac{\Delta^2}{3}\right]^{\frac{1}{2}}} (1-\delta)\, N_u \frac{\Delta}{1+\Delta} \hat{\Phi} \frac{f}{1-\delta} \quad \ldots (61)$$

Inserting the value of $I_{rms}\, N_u$ from Appendix 1 (Eq.30) in Eq.61:

$$P_o = \left[\frac{P_w\, A_w\, F_w\, U_F}{\rho_c\, m\, l_w\, F_R}\right]^{\frac{1}{2}} \hat{\Phi} f \frac{\Delta}{1+\Delta} \cdot \frac{\sqrt{2}}{\left[1 + \frac{\Delta^2}{3}\right]^{\frac{1}{2}}}. \quad \ldots (62)$$

For a two-winding transformer, U_F is equal to 1, and P_o is given by:

$$P_o = \left[\frac{P_w\, A_w\, F_w}{\rho_c\, m\, l_w\, F_R}\right]^{\frac{1}{2}} \hat{\Phi} f \frac{\Delta}{1+\Delta} \cdot \frac{\sqrt{2}}{\left[1 + \frac{\Delta^2}{3}\right]^{\frac{1}{2}}}. \quad \ldots (62)$$

For a three-winding transformer in which one-third of the winding space is occupied by an extra winding to limit the transistor collector voltage should the load be removed, U_F is equal to $\frac{2}{3}$, and P_o is given by:

$$P_o = \left[\frac{P_w\, A_w\, F_w}{\rho_c\, m\, l_w\, F_R}\right]^{\frac{1}{2}} \hat{\Phi} f \frac{\Delta}{1+\Delta} \cdot \frac{1}{\left[1 + \frac{\Delta^2}{3}\right]^{\frac{1}{2}}} \frac{2}{\sqrt{3}}. \quad \ldots (63)$$

For a simple flyback (or ringing-choke) converter in which the stored energy in the transformer is reduced to zero at the end of every cycle,

$$\Delta = 1,$$

and

$$\frac{\Delta}{1+\Delta} \cdot \frac{1}{\left[1 + \frac{\Delta^2}{3}\right]^{\frac{1}{2}}} = \frac{\sqrt{3}}{4}. \quad \ldots (64)$$

Hence for a two-winding transformer:

$$P_o = \left[\frac{P_w\, A_w\, F_w}{\rho_c\, m\, l_w\, F_R}\right]^{\frac{1}{2}} \hat{\Phi} f \frac{\sqrt{3}}{2\sqrt{2}}, \quad \ldots (65)$$

and for the three-winding transformer with a voltage-limiting winding occupying one-third of the winding space:

$$P_o = \left[\frac{P_w\, A_w\, F_w}{\rho_c\, m\, l_w\, F_R}\right]^{\frac{1}{2}} \hat{\Phi} f \frac{1}{2}. \quad \ldots (66)$$

APPENDIX 5

Chokes for Forward and Push-pull Converters

The current and flux waveforms of output chokes in forward and push-pull converters are of the same form as those shown in Figs.19 and 20. Therefore, if the power supply d.c. output current is equal to I_o, from Eq.54 in Appendix 4 the r.m.s. current in the choke is given by:

$$I_{rms} = I_o \left[1 + \frac{\Delta^2}{3}\right]^{\frac{1}{2}}, \quad \ldots (67)$$

where

$$\Delta = \frac{I_o min}{I_o max},$$

and $I_o min$ is the minimum value of I_o which will keep the rectifiers feeding the choke in continuous conduction, and so maintain good regulation of the output voltage with changes of load current. Note that for push-pull converters, a further minimum component of output current is required to prevent the rectifiers being turned off by transformer magnetising current, and:

$$I_o min_{total} = I_o min_{ch} + I_o min_{tr}.$$

From Eq.67:

$$I_o = \frac{I_{rms}}{\left[1 + \frac{\Delta^2}{3}\right]^{\frac{1}{2}}}. \quad \ldots (68)$$

From Fig.20:

$$\text{total flux change} = 2\Delta\, \Phi mean,$$

$$= 2\Delta \frac{\hat{\Phi}}{1+\Delta}, \quad \ldots (69)$$

where $\hat{\Phi}$ is the peak value.

The voltage across the choke during the interval $(1-\delta)$ T (shown in Fig.20) is V_o, the power supply output voltage (ignoring rectifier volt-drop). Therefore, using the expression:

$$V = N \frac{d\Phi}{dt},$$

the output voltage V_o is given by:

$$V_o = 2N_u \frac{\Delta}{1+\Delta} \hat{\Phi} \frac{1}{(1-\delta)T}. \quad \ldots (70)$$

For a forward converter, cycle time T is equal to 1/f. For a push-pull converter, T is equal to 1/2f. For a choke:

$$(V_i - V_o)\,\delta\,T = V_o\,(1-\delta)\,T. \qquad \ldots(71)$$

Therefore:

$$\delta = \frac{V_o}{V_i}, \qquad \ldots(72)$$

where V_o is the power supply output voltage and V_i is the input voltage referred to the choke input terminal.

For a forward converter:

$$V_o = \frac{V_i min}{2}, \qquad \ldots(73)$$

when δ is equal to 0·5. For a push-pull converter:

$$V_o = V_i min, \qquad \ldots(74)$$

when δ is equal to 1.

Therefore, for a forward converter:

$$(1-\delta)\,T = \left(1-\frac{V_o}{V_i}\right)T,$$

$$= \left(1-\frac{V_i min}{2V_i}\right)\frac{1}{f},$$

$$= \left(2-\frac{V_i min}{V_i}\right)\frac{1}{2f}. \qquad \ldots(75)$$

For a push-pull converter:

$$(1-\delta)\,T = \left(1-\frac{V_o}{V_i}\right)T,$$

$$= \left(1-\frac{V_i min}{V_i}\right)\frac{1}{2f}, \qquad \ldots(76)$$

and so:

$$(1-\delta)\,T = \left(K_1-\frac{V_i min}{V_i}\right)\frac{1}{2f}, \qquad \ldots(77)$$

where K_1 is equal to 1 for a push-pull converter, and equal to 2 for a forward converter. Therefore,

$$V_o = 2N_u\,\frac{\Delta}{1+\Delta}\,\hat{\Phi}\,\frac{1}{\left(K_1-\frac{V_i min}{V_i}\right)\frac{1}{2f}},$$

$$= 4N_u\,\frac{\Delta}{1+\Delta}\,\hat{\Phi}f\,\frac{1}{\left(K_1-\frac{V_i min}{V_i}\right)} \qquad \ldots(78)$$

Power-handling capability P_o is equal to $I_o V_o$, therefore:

$$P_o = \frac{I_{rms}}{\left[1+\frac{\Delta^2}{3}\right]^{\frac{1}{2}}}\,4N_u\,\frac{\Delta}{1+\Delta}\,\hat{\Phi}f\,\frac{1}{\left(K_1-\frac{V_i min}{V_i}\right)}. \qquad \ldots(79)$$

Inserting the value of $I_{rms}\,N_u$ from Appendix 1 (Eq.30) in Eq.79:

$$P_o = \left[\frac{P_w\,A_w\,F_w\,U_F}{\rho_c\,m\,l_w\,F_R}\right]^{\frac{1}{2}}\hat{\Phi}f\,4\,\frac{\Delta}{1+\Delta}\times$$

$$\times\ \frac{1}{\left[1+\frac{\Delta^2}{3}\right]^{\frac{1}{2}}}\cdot\frac{1}{\left(K_1-\frac{V_i min}{V_i}\right)}. \qquad \ldots(80)$$

For a choke, U_F is equal to 1, and P_o is minimum when V_i is maximum. Therefore:

$$P_o = \left[\frac{P_w\,A_w\,F_w}{\rho_c\,m\,l_w\,F_R}\right]^{\frac{1}{2}}\hat{\Phi}f\,4\,\frac{\Delta}{1+\Delta}\times$$

$$\times\ \frac{1}{\left[1+\frac{\Delta^2}{3}\right]^{\frac{1}{2}}}\cdot\frac{1}{\left(K_1+\frac{V_i min}{V_i max}\right)}, \qquad \ldots(81)$$

in which K_1 is equal to 1 for a push-pull converter, and equal to 2 for a forward converter.

APPENDIX 6

Push-pull Converter Transformer Limited by Magnetising Current

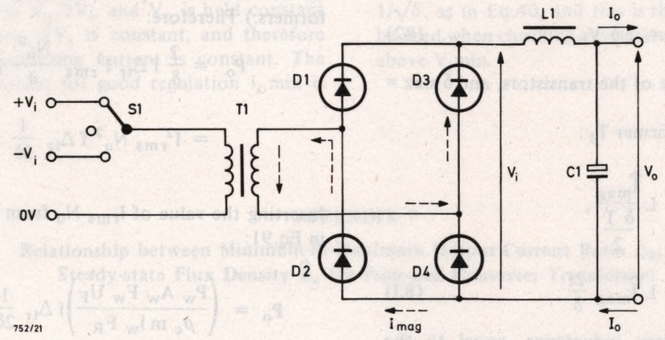


Fig.21 — Transformer in push-pull converter with bridge-rectified output

As shown in Ref.2, push-pull converters maintain a nearly-constant output voltage for a fixed duty cycle δ and a fixed supply voltage, provided that the current in the output choke exceeds the transformer peak magnetising current referred to the secondary. For choke currents in excess of the transformer magnetising current, the d.c. output voltage can be held constant by small variations of δ which are required only to counteract circuit losses.

To maintain good output voltage regulation, the d.c. output current must exceed a minimum value given by:

$$I_o min_{total} = I_o min_{tr} + I_o min_{ch},$$

where $I_o min_{tr}$ and $I_o min_{ch}$ are the components of minimum output current determined by the transformer and by the choke (see Appendix 5 for calculation of $I_o min_{ch}$).

Fig.21 shows a two-winding transformer used in a push-pull converter with a bridge-rectified output. Fig.22a shows the voltage waveform at the choke input terminal, and this waveform determines the d.c. output voltage V_o. The voltage across the transformer secondary is shown in Fig.22b. The switch S_1 in Fig.21 represents the switching transistors. While switch S_1 is in the open-circuit (centre) position, the transformer magnetising current I_{mag} (shown dashed in Fig.22b) must flow through two of the output diodes D_2 and D_3 as indicated in Fig.21. Provided that I_o exceeds $\hat{I}_{mag}$, diodes D_1 and D_4 will be forced to conduct, and with all four diodes conducting the transformer secondary voltage must be zero, giving the desired voltage waveform as indicated.

Neglecting the voltage drop across the diodes for the purpose of calculating transformer output power, and

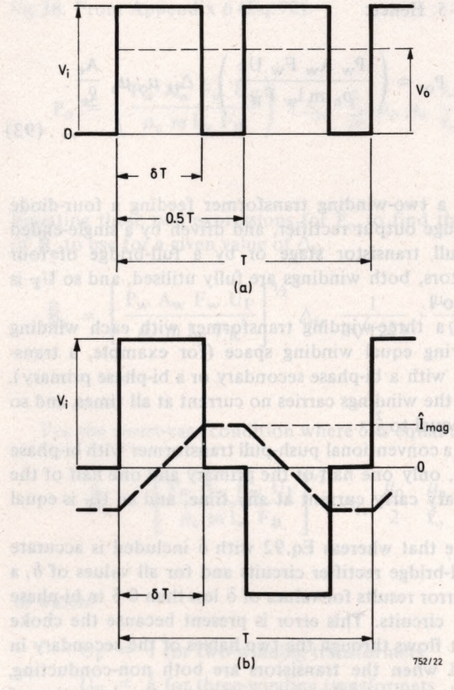


Fig.22 — Waveforms of (a) choke input voltage, and (b) transformer voltage and magnetising current

considering the voltage across the choke inductance under steady-state operating conditions:

$$(V_i - V_o)\,\delta\,T = V_o\,(0{\cdot}5 - \delta)\,T.$$

Therefore:

$$V_o = 2\delta\,V_i, \qquad \ldots(82)$$

where δ is the duty cycle of the transistors, and δmax = 0·5.

Considering the transformer T_1:

$$V_i = L\frac{\hat{I}_{mag}}{\frac{\delta\,T}{2}},$$

$$= L\,\hat{I}_{mag}\,\frac{2f}{\delta}, \qquad \ldots(83)$$

where L is the secondary inductance, equal to the primary inductance.

Therefore:

$$V_o = 2\delta\,L\,\hat{I}_{mag}\,\frac{2f}{\delta},$$

$$= 4\,f\,L\,\hat{I}_{mag}. \qquad \ldots(84)$$

Replacing $\hat{I}_{mag}$ with $\Delta_{tr}\,I_o$, which is the minimum component of d.c. output current required to prevent turn-off of the output diodes by $\hat{I}_{mag}$:

$$V_o = 4\,f\,L\,\Delta_{tr}\,I_o, \qquad \ldots(85)$$

and

$$P_o = V_o\,I_o,$$

$$= 4\,f\,L\,\Delta_{tr}\,I_o^2. \qquad \ldots(86)$$

The r.m.s. current in primary and secondary windings (ignoring magnetising current) is given by:

$$I_{rms} = \left[I_o^2\,\frac{\delta}{0{\cdot}5}\right]^{\frac{1}{2}}. \qquad \ldots(87)$$

Therefore:

$$I_o^2 = \frac{0{\cdot}5}{\delta}\,I^2_{rms}, \qquad \ldots(88)$$

and so:

$$P_o = 4\,f\,L\,\Delta_{tr}\,\frac{0{\cdot}5}{\delta}\,I^2_{rms},$$

$$= \frac{2}{\delta}\,f\,L\,\Delta_{tr}\,I^2_{rms}. \qquad \ldots(89)$$

The transformer secondary inductance L is given by:

$$L = N^2\,\mu_o\,\mu_a\,\frac{A_e}{\ell_e}, \qquad \ldots(90)$$

where

$$N = \frac{N_u}{2}.$$

(As stated in Appendices 2 and 4, practical turns ratios do not affect the power-handling capability of transformers.) Therefore:

$$P_o = \frac{2}{\delta}\,f\,\Delta_{tr}\,I^2_{rms}\,\frac{N_u^2}{4}\,\mu_o\,\mu_a\,\frac{A_e}{\ell_e},$$

$$= I^2_{rms}\,N_u^2\,f\,\Delta_{tr}\,\frac{1}{2\delta}\,\mu_o\,\mu_a\,\frac{A_e}{\ell_e}. \qquad \ldots(91)$$

Inserting the value of $I_{rms}\,N_u$ from Appendix 1 (Eq.30) in Eq.91:

$$P_o = \left(\frac{P_w\,A_w\,F_w\,U_F}{\rho_c\,m\,l_w\,F_R}\right) f\,\Delta_{tr}\,\frac{1}{2\delta}\,\mu_o\,\mu_a\,\frac{A_e}{\ell_e}. \qquad \ldots(92)$$

Because P_o will be minimum (or maximum temperature rise will occur) when δ is at its maximum value of 0·5, the term $(1/2\delta)$ can be omitted. This term should, of course, be taken into account when comparing theoretical and measured temperature rises with δ less than 0·5. Hence:

$$P_o = \left(\frac{P_w\,A_w\,F_w\,U_F}{\rho_c\,m\,l_w\,F_R}\right) f\,\Delta_{tr}\,\mu_o\,\mu_a\,\frac{A_e}{\ell_e}. \qquad \ldots(93)$$

For a two-winding transformer feeding a four-diode full-bridge output rectifier, and driven by a single-ended push-pull transistor stage or by a full-bridge of four transistors, both windings are fully utilised, and so U_F is equal to 1.

For a three-winding transformer with each winding occupying equal winding space (for example, a transformer with a bi-phase secondary or a bi-phase primary), one of the windings carries no current at all times, and so U_F is equal to $\frac{2}{3}$.

For a conventional push-pull transformer with bi-phase output, only one half of the primary and one half of the secondary carry current at any time, and so U_F is equal to $\frac{1}{2}$.

Note that whereas Eq.92 with δ included is accurate for full-bridge rectifier circuits and for all values of δ, a small error results for values of δ less than 0·5 in bi-phase output circuits. This error is present because the choke current flows through the two halves of the secondary in parallel when the transistors are both non-conducting, and this was not taken into account in the derivation of the r.m.s. current in the windings. The error can normally be neglected, however, because P_o will normally be assessed for a value of δ equal or close to 0·5.

Note also that Eq.92 could be very easily misinterpreted when assessing P_o for a given temperature rise at supply voltages other than $V_i$min, where δ is equal to 0·5, because in a power supply where the frequency and the transformer inductance have been fixed, Δ_{tr} is a function of δ.

Since δ is equal to $V_o/2V_i$, and V_o is held constant by the feedback loop, δV_i is constant, and therefore the transformer magnetising current is constant. The minimum output current for good regulation $I_o$min is equal to the magnetising current, and so $I_o$min is also constant, and $P_o$min for the transformer is constant. From Appendix 2 (Eq.40), P_o is proportional to $1/\sqrt{\delta}$. Therefore Δ_{tr} (= $P_o$min/P_o) is proportional to $\sqrt{\delta}$.

Replacing Δ_{tr} in Eq.93 by $K_2\sqrt{\delta}$ (where K_2 is an arbitrary constant), P_o is seen to be proportional to $1/\sqrt{\delta}$, as in Eq.40, and this is the relationship that must be used when checking temperature rise at supply voltages above $V_i$min.

APPENDIX 7

Relationship between Minimum-to-Maximum Output Current Ratio Δ_{tr} and Steady-state Flux Density $\hat{B}_e$ for Push-pull Converter Transformer

From Appendix 2 (Eq.38):

$$P_o = \left[\frac{P_w\,A_w\,F_w\,U_F}{\rho_c\,m\,l_w\,F_R}\right]^{\frac{1}{2}}\hat{B}_e\,A_e\,f\sqrt{(2/\delta)},$$

where $\hat{B}_e\,A_e$ has been inserted for the value of $\hat{\Phi}$ in Eq.38. From Appendix 6 (Eq.92):

$$P_o = \left(\frac{P_w\,A_w\,F_w\,U_F}{\rho_c\,m\,l_w\,F_R}\right) f\,\Delta_{tr}\,\frac{1}{2\delta}\,\mu_o\,\mu_a\,\frac{A_e}{\ell_e}.$$

Equating these two expressions for P_o to find the value of $\hat{B}_e$ to use for a given value of Δ_{tr}:

$$\hat{B}_e = \left[\frac{P_w\,A_w\,F_w\,U_F}{\rho_c\,m\,l_w\,F_R}\right]^{\frac{1}{2}}\Delta_{tr}\,\frac{1}{2\sqrt{(2\delta)}}\cdot\frac{\mu_o\,\mu_a}{\ell_e}. \qquad \ldots(94)$$

For the worst-case condition where δ is equal to 0·5:

$$\hat{B}_e = \left[\frac{P_w\,A_w\,F_w\,U_F}{\rho_c\,m\,l_w\,F_R}\right]^{\frac{1}{2}}\Delta_{tr}\,\frac{\mu_o}{2}\cdot\frac{\mu_a}{\ell_e}, \qquad \ldots(95)$$

in which:

U_F = 1 for two-winding transformers,
U_F = $\frac{2}{3}$ for three-winding transformers (bi-phase primary or secondary),
U_F = $\frac{1}{2}$ for four-winding transformers (bi-phase primary and secondary).

To find Δ_{tr} for a given value of $\hat{B}_e$:

$$\Delta_{tr} = \hat{B}_e\,\frac{2}{\mu_o}\cdot\frac{\ell_e}{\mu_a}\cdot\frac{1}{\left[\frac{P_w\,A_w\,F_w\,U_F}{\rho_c\,m\,l_w\,F_R}\right]^{\frac{1}{2}}}. \qquad \ldots(96)$$

The term X can be substituted in Eq.96 from Eq.2, where:

$$X = \left[\frac{P_w\,A_w\,F_w}{\rho_c\,m\,l_w\,F_R}\right]^{\frac{1}{2}},$$

and inserting the value of μ_o:

$$\Delta_{tr} = \frac{\hat{B}_e}{X}\cdot\frac{\ell_e}{\mu_a}\cdot\frac{10^7}{2\pi}\cdot\frac{1}{\sqrt{U_F}}.$$

Inserting the term Z, evaluated in Table 1:

$$\Delta_{tr} = \frac{\hat{B}_e}{X}\cdot\frac{\ell_e}{\mu_a}\cdot\frac{10^7}{2\pi}\cdot\frac{1}{\frac{Z}{2}},$$

$$= \frac{\hat{B}_e}{XZ}\cdot\frac{\ell_e}{\mu_a}\cdot\frac{10^7}{\pi},$$

or

$$\Delta_{tr} = \frac{\hat{\Phi}}{XZ}\cdot\frac{\ell_e}{A_e}\cdot\frac{1}{\mu_a}\cdot\frac{10^7}{\pi}. \qquad \ldots(97)$$

In addition:

$$Pmin_{tr} = \Delta_{tr}\,P_o,$$

$$= \Delta_{tr}\,XYZ,$$

and since from Eq.3, Y is equal to $\hat{\Phi}$f:

$$Pmin_{tr} = \hat{\Phi}^2\,\frac{\ell_e}{A_e}\cdot\frac{f}{\mu_a}\cdot\frac{10^7}{\pi}. \qquad \ldots(98)$$

APPENDIX 8

Relationship between Core Loss P_c and Winding Loss P_w for Maximum Efficiency

The power-handling capability P_o is given by:

$$P_o = \left[\frac{P_w\, A_w\, F_w}{\rho_c\, m\, l_w\, F_R}\right]^{\frac{1}{2}} \hat{B}_e\, A_e\, f\, Z, \quad \ldots (99)$$

where Z is evaluated in Table 1, and $(\hat{B}_e\, A_e)$ is used for the value of $\hat{\Phi}$.

The core loss (ignoring eddy-current) can be expressed by:

$$P_c = K_3\, f\, (K_4\, \hat{B}_e)^n\, V_e, \quad \ldots (100)$$

where K_3 and K_4 are constants, and n is the Steinmetz exponent. Therefore:

$$\hat{B}_e = \left[\frac{P_c}{K_3\, f\, V_e}\right]^{\frac{1}{n}} \frac{1}{K_4},$$

and so:

$$P_o = \left[\frac{A_w\, F_w}{\rho_c\, m\, l_w\, F_R}\right]^{\frac{1}{2}} A_e\, f\, Z\, \left[P_t - P_c\right]^{\frac{1}{2}} \times$$

$$\times \left[\frac{P_c}{K_3\, f\, V_e}\right]^{\frac{1}{n}} \frac{1}{K_4}. \quad \ldots (101)$$

For maximum P_o:

$$[P_t - P_c]^{\frac{1}{2}}\, P_c^{\frac{1}{n}} \quad \ldots (102)$$

must be maximum. Therefore:

$$P_t\, P_c^{\frac{2}{n}} - P_c\left(1 + \tfrac{2}{n}\right) \quad \ldots (103)$$

must be maximum, and therefore:

$$\frac{d}{dP_c}\left\{P_t\, P_c^{\frac{2}{n}} - P_c\left(1 + \tfrac{2}{n}\right)\right\} = 0, \quad \ldots (104)$$

$$P_t\, \frac{2}{n}\, P_c\left(\tfrac{2}{n} - 1\right) - \left(1 + \frac{2}{n}\right) P_c^{\frac{2}{n}} = 0, \quad \ldots (105)$$

and

$$P_{t_,} = \frac{n}{2}\, \frac{\left(1 + \frac{2}{n}\right) P_c^{\frac{2}{n}}}{P_c\left(\frac{2}{n} - 1\right)},$$

$$= \frac{n}{2}\, \frac{n+2}{n}\, P_c,$$

$$= \left(1 + \frac{n}{2}\right) P_c. \quad \ldots (106)$$

Core loss P_c is given by:

$$P_c = \frac{P_t}{1 + \frac{n}{2}}, \quad \ldots (107)$$

and winding loss P_w is given by:

$$P_w = P_t - P_c,$$

$$= \left(1 + \frac{n}{2}\right) P_c - P_c,$$

$$= \frac{n}{2}\, P_c. \quad \ldots (108)$$

When n is equal to 2, as for A9 ferrite material:

$$P_w = P_c,$$

$$= \frac{P_t}{2}. \quad \ldots (109)$$

When n is equal to 2·5, as for A16 (3C8) material:

$$P_c = \frac{P_t}{1 + \frac{2{\cdot}5}{2}},$$

$$= \frac{P_t}{2{\cdot}25}, \quad \ldots (110)$$

$$= 0{\cdot}444\, P_t;$$

and

$$P_w = \frac{2{\cdot}5}{2}\, P_c, \quad \ldots (111)$$

$$= 0{\cdot}555\, P_t.$$